Coated Conductor Development Roadmapping Workshop II

Bridging the Gap Between Tape Fabrication and Cable Manufacturing to Meet Customer Needs

Workshop Proceedings

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Superconductivity for Electric Systems Program

Office of Electric Transmission and Distribution
U.S. Department of Energy

Prepared by:
Energetics, Incorporated

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Table of Contents

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1. SUMMARY

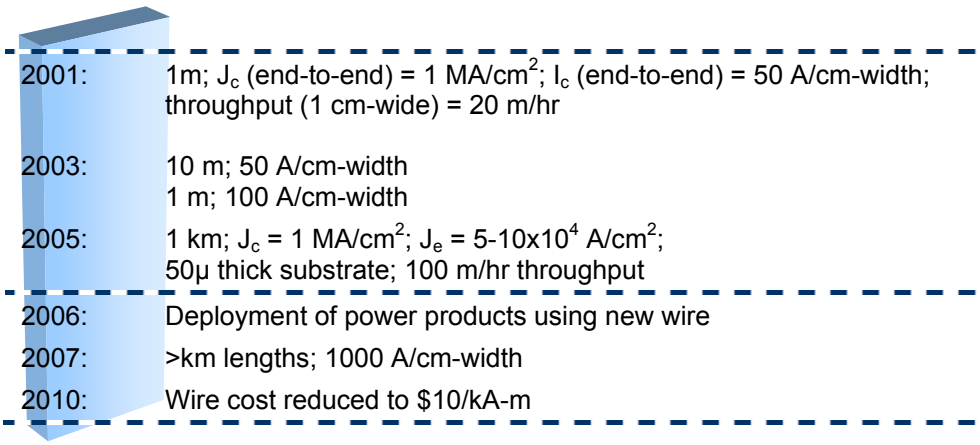
1.1 Background and Purpose

In January 2001, the U.S. Department of Energy held a two-day facilitated workshop aimed at defining a future research agenda to evaluate, demonstrate, and accelerate processing, fabrication, and manufacturing of high-temperature superconducting (HTS) coated conductors that would meet the needs of the U.S. electric power industry. This workshop resulted in the *Coated Conductor Technology Development Roadmap: Priority Research and Development Activities Leading to Economical Commercial Manufacturing*, August 2001, (see www.ornl.gov/HTS/pdf/CCRoadmap8-23.PDF). The roadmap updates the November 1997 report, *Research and Development Roadmap to Achieve Electrical Wire Advancements from Superconducting Coatings*.

The 2001 roadmap presents the priority R&D needs in the following activity areas:

- Fabrication Pathways
- Substrate Development and Characterization
- Simplified Buffer Layer Architecture
- Improved YBCO Quality
- Faster Deposition Rates
- Process Monitoring and Control Strategies/Methods
- Production Scale-Up
- End-User Applications

The 2001 roadmap considers the time period of 2001 through 2005. *Performance targets* (at 77K) developed at the workshop are as follows:



The highest priorities identified are: increasing HTS film thickness while maintaining high current density and increasing film deposition rates or mass throughput while maintaining quality.

Roadmap targets for 2005 are:

- Accelerate Development of Existing Fabrication Technology
- Develop New Approaches/Alternative Fabrication Techniques
- Substrate Development and Characterization
  - Substrate cost $1/m, stronger, thinner, non-magnetic
  - Continuous texturing systems, >100m lengths
  - On-line diagnostics before HTS deposition
- Simplified Buffer Layer Architecture
  - Non-vacuum processing
  - No buffer approaches
  - Dual side coatings
- Improved YBCO Quality
  - Defects and causes
  - Current limiting mechanisms >1 km
  - 500 A/cm-width (77K, self-field)
- Faster Deposition Rates
  - Enhance PLD and other vapor deposition process efficiency by 5-10 X
  - Rate: 100m/hr/1 cm-width; $\geq$500A

In late October 2002, a German research group reported that they had produced a 10 m IBAD-YSZ tape with a J_c = 2.23 MA/cm^2, I_c (end-to-end) = 223 A/cm-width (at 77K). These tapes were prepared on a 50-100 micron nonmagnetic stainless steel ribbon, using a textured YSZ, IBAD buffer layer (1.3-1.5 micron thick), 1-3 micron layer of YBCO, and a gold protective layer. They employed a high-rate PLD process, with volumetric coating rates of 60-70 nm-m^2/hr.

In early December 2002, U.S. companies reported that they had exceeded the DOE goals. SuperPower achieved I_c values above 100 A/cm-width end-to-end for a 10 m tape at 77K produced by the IBAD-MOCVD tape process. American Superconductor also achieved I_c values above 100 A/cm-width end-to-end for a 10 m tape using RABiTS-MOD (BaF_2) process. These accomplishments exceeded the DOE December 2003 performance targets. This accelerated progress has made it necessary to revisit and update the 2001 roadmap.

DOE is now starting the process of developing a new roadmap that builds on prior efforts and incorporates the latest achievements in **continuous processing of HTS coated conductors.** This new roadmap will focus on defining R&D priorities and pathways to achieve the vision of a commercially suitable final conductor configuration and assembly. New ways will be explored for the national laboratories, academia, and

private companies to work directly together to accelerate technology transfer and product development. **In this technology roadmapping workshop, you will help identify the R&D activities, priorities, and pathways for achieving the Vision.**

The efforts of this workshop will result in the new *HTS Coated Conductor Development Roadmap* that will link the broadly defined targets outlined in the vision with a detailed research agenda of near- and mid-term R&D activities addressing technology needs of the electric power industry. When the roadmap is published, implementation through collaborative research partnerships composed of private companies, government agencies, academia , and private research institutions will help the *Vision* become reality.

1.2 Vision

Low-cost, high-performance HTS Coated Conductors will be available in 2005 in hundreds of meter lengths. For applications in liquid nitrogen, the wire price will be less than $50/kA-m, while for applications requiring cooling to temperatures of 20-60K the price will be less than $30/kA-m. By 2010, the price-performance ratio will have improved for kilometer lengths by at least a factor of five.

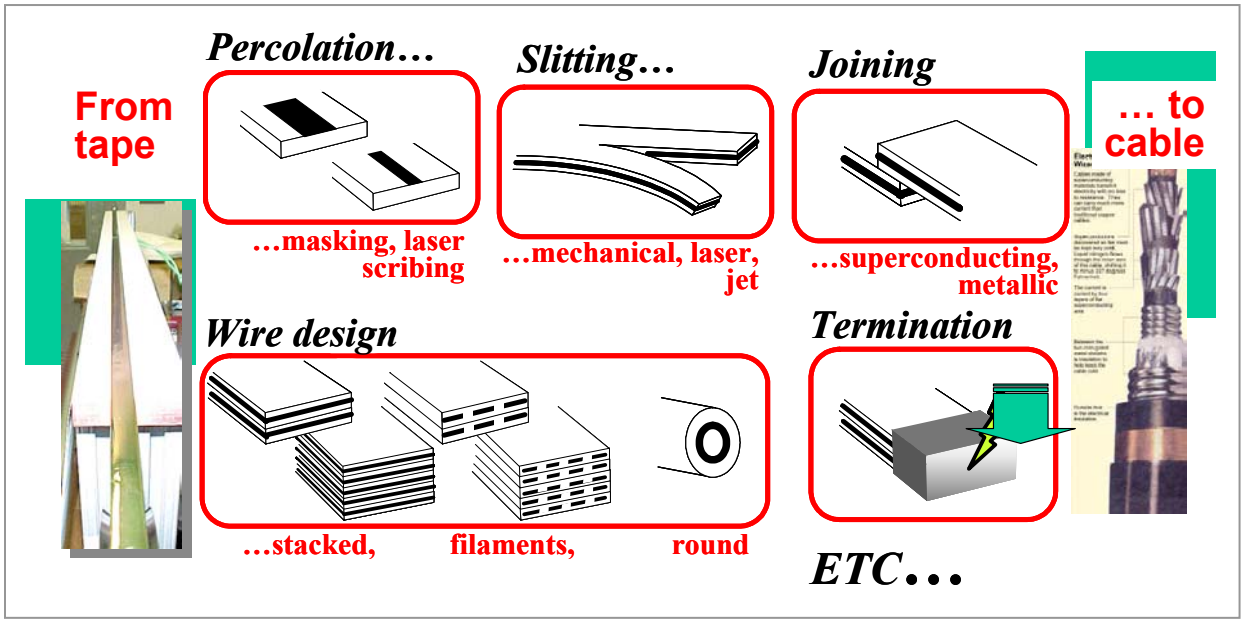
HTS wires based upon coatings of YBCO on textured, buffered metallic substrates will offer unprecedented current carrying capacity at high temperatures and in the presence of strong magnetic fields. Coated conductors also will be fabricated using industry scalable deposition technologies, many of which are presently in use in the semiconductor and photographic film industries, but which have not been adapted for use in **continuous processing** of the templates or superconductor layers.

The HTS industry will work with national laboratories to develop high-performance, low-cost, HTS coated conductor wire. Specific national laboratories have developed cutting edge research facilities where industry researchers can work collaboratively with national laboratory scientists. This partnering arrangement is designed to accelerate development and private sector application of HTS coated conductor wires. These partnerships will also enable faster scale-up of discoveries in materials laboratory processes that give unprecedented ability to carry large electric currents. A performance measure is achieving industry production of kilometer lengths of HTS coated conductor wire by 2010. Beyond this, present work will focus on cooperative national laboratory/private company research intended to reproducibly fabricate 100-meter lengths of wire that carry over 300 amps in single strands.

The U.S. will maintain its leadership position in HTS coated conductor development. U.S. industry will apply HTS devices to address critical issues in the nation's long-term energy strategy.

1.3 Conductor Design and Engineering Issues

This workshop focused on bridging the gap between tape fabrication and cable manufacturing.



Workshop participants were asked to identify and discuss HTS conductor design and engineering activities between now and 2010. These activities will form R&D pathways that will ultimately:

- Resolve issues limiting application of today's HTS industry-manufactured coated conductor by developing a detailed understanding of materials properties and limitations relevant to specific applications
- Reduce the alternating current losses in half compared with today's geometry
- Demonstrate commercial availability, through U.S. industry partners, of coated conductors in forms engineered for magnets and cables
- Develop conductor and "building block" designs that will enable full implementation with HTS cables, transformers, and generators
- Integrate engineered conductors with balance of system – cryogenics, electronics.

Initial coated conductor design and engineering issues are:

- Adhesion of coatings at low temperature
- Cross-sectional architecture for reinforcing tapes
- All tape mechanical properties unknown except longitudinal tension
- All epoxy-impregnated coil properties unknown
- Splicing method and properties of splices not known
- Slitting methods and properties of substrates and YBCO conductors not known
- Shock tolerance and strain rate effects not known

- Long-term performance (degradation over time) not known
- Coil dynamic testing capability needed
- Definition and basic modeling of "building block" characteristics needed

It is clear that a strong coordinated effort is needed to overcome the barriers to continuous processing of high quality, low cost HTS coated conductors and production scale-up that will lead to industrial-scale commercial manufacturing.

1.4 Workshop Format and Agenda

The workshop was a 1½ day facilitated meeting that took place July 28-29, 2003 at the Loew L'Enfant Plaza Hotel in Washington, DC. The workshop brought together respected experts from various segments of the industry and others that are involved in developing processes to fabricate finished wire products and devices using advanced HTS materials. Invited participants represented a cross-section of companies that produce HTS wire as well as companies that are likely to use HTS wire, researchers, and government programs. The workshop focused on technical solutions to major material and processing challenges. It included a plenary session, facilitated working sessions, and a summary session. The Agenda can be found at the end of this section.

During the breakout sessions, each group was asked to review the technical barriers and select the most critical challenges to achieving the vision. Participants were asked to share their thoughts on what the "final" conductor configurations should look like in order to satisfy the vision. This will help to define the final conductor as the goal of the roadmap. Participants identified and ranked needed R&D activities. These activities were categorized as near- and mid-term time frames and linked as appropriate (e.g., R&D that must be completed before other R&D can begin). For the high-priority R&D activities, the appropriate role of the national laboratories, private companies, and universities were discussed.

Specific Workshop Objectives

- Assess the performance goals for the various components of coated conductors, i.e., the metallic substrate, buffer layers, YBCO coating, and any additional components needed for stable conductor operation.
- Develop a consensus of the critical research needs and determine the improvements needed for processing methods to meet performance goals.
- Focus on solving "problems" that slow progress toward meeting the performance goals and identify opportunities for cooperation between industry and government.
- Define pathways to transform coated conductors from laboratory-scale development to real-world commercial conductors. Identify key opportunities to scale-up existing coated conductor technology to commercially-attractive manufacturing processes.

COATED CONDUCTOR TECHNOLOGY DEVELOPMENT ROADMAP II

BRIDGING THE GAP BETWEEN TAPE FABRICATION AND CABLE MANUFACTURING TO MEET CUSTOMER NEEDS

FINAL AGENDA

Loews L'Enfant Plaza, Washington, DC

MONDAY, JULY 28, 2003

TIME	SESSION
7:30 – 8:30 am	Registration and Continental Breakfast
8:30 – 10:30 am	**Plenary Session** ♦ Welcome & Introduction – J. Daley, DOE ♦ Vision ♦ Thought Provoking Perspectives on HTS Coated Conductor Product Needs - David Larbalestier, U of Wisconsin, Madison - John Scudiere, AMSC - Venkat Selvamanickman, SuperPower - Ken Marken, OST - David Lindsay, ULTERA ♦ Workshop Process and Expectations – J. Badin, Energetics
10:30 – 11:00 am	Break
11:00 – 12:00 pm	Plenary Session *(continued)*
12:00 – 1:15 pm	Luncheon
1:15 – 5:30 pm	**Breakout Sessions** - Defining the Vision-Achieving Conductor - Break (3:00 – 3:30 pm) - R&D Activities to Achieve the Vision
6:00 pm	Reception

TUESDAY, JULY 29, 2003

TIME	SESSION
7:30 – 8:00 am	Continental Breakfast
8:00 – 10:30 am	**Breakout Sessions** *(continued)* - Actions and Timeframes
10:30 – 10:45 am	Break
10:45 – 12:00 pm	**Plenary Summary Session** - Findings of Breakout Sessions and Concluding Remarks
12:00 pm	**Adjourn**

1.5 What Comes Next?

The focus of the workshop was on continuous processing and manufacturing scale-up of HTS coated conductors. The results of this workshop will help establish a comprehensive technology agenda that will be used to guide future research initiatives and partnerships. Discussions covered a wide spectrum of non-proprietary research needs and opportunities. Some research may be best pursued by equipment developers and manufacturers, some is appropriate for industry collaborations with universities, and some is best suited for industry-government partnerships. Participants were encouraged to seek new opportunities for R&D collaboration. Creative ideas were sought.

The results of the workshop will be used to:

- Revise performance targets for each government fiscal year beginning with 2004
- Confirm or modify critical material and processing challenges and limitations to achieving the vision for continuous processing of HTS coated conductors
- Identify key opportunities to scale-up existing coated conductor technology to commercially-attractive manufacturing processes
- Reach a consensus of the priority research needs
- Develop near- and mid-term R&D activities
- Identify interrelationships between R&D activities
- Make recommendations for an optimum R&D portfolio
- Identify opportunities for cooperation among the industry, academia, and the government to overcome key materials and process related challenges.

The efforts of this workshop will result in an updated *HTS Coated Conductor Development Roadmap* that will link the broadly defined targets outlined in the vision with a detailed research agenda of short-, mid-, and long-term R&D activities addressing technology needs of the electric power industry. When the roadmap is published, implementation through collaborative research partnerships composed of private companies, government agencies, academia, and private research institutions will help the *Vision* become a reality.

2. Discussion Groups

2.1 Organization and Focus Questions

The workshop was designed as a product-oriented meeting in which participants have active roles. The four breakout sessions consisted of:

1. **Substrates/Buffers**
2. **RE-123 Nucleation, Growth, and Flux Pinning**
3. **&4 Conductor Design and Engineering (A&B)** (ac losses, stability, quench protection, conductor geometry, cost-effective manufacturing)

Breakout sessions 3 and 4 covered the same scope and were held concurrently. The outcome of this workshop was to identify the most critical issues and activities for an R&D program that will develop and transfer successful coated conductor technologies. We also hoped to identify novel approaches that if successful would have revolutionary impact.

Breakout Group 1: Substrates/Buffers

Fabrication of a coated conductor requires an integrated material system including the substrate, buffer/template layer and superconductor. This integrated system must achieve a microstructure that leads to the necessary superconducting performance. Deposition approaches capable of achieving such integrated systems at an economical cost must be developed to meet a variety of expected coated conductor applications. While remarkable success has been achieved recently, basic material science studies will be necessary to create optimized buffer/template layers and optimized, tailored conductors. Specific issues include surface finish requirements, strength and magnetism, process speed, and stress-related issues. Participants considered the following:

- What would be the most difficult aspect of the process to scale-up to long lengths of 100 m?
- What would be the most difficult aspect of the process to scale-up to widths of several centimeters followed at some point in the processing by a slitting operation?
- What R&D areas do you think need to be pursued to make this technology viable?

Breakout Group 2: RE-123 Nucleation, Growth, and Flux Pinning

Various approaches to the growth of the superconducting layer in a coated conductor have been demonstrated. This has occurred, however, on the basis of a limited understanding of the growth mechanism and phase stability of the YBCO conductor. Optimization of the superconductor for the various applications will require a firm understanding of how to develop the needed microstructure consistent with economical, well controlled growth processes. Uniformity and reproducibility of superconducting properties in coated conductors need to be achieved. Specific issues include:

- What controls the microstructure?
- What are the effects of high deposition rates?
- Do liquid fluxes play a role in the YBCO growth?
- What chemical additions or substitutions in YBCO might be beneficial?
- Effect of the interface with the epi-buffer layer on the YBCO?
- How can we achieve the needed level of deposition control?
- The properties of YBCO dependent on the deposition process/method?

Flux pinning in coated conductors has been one of the major thrusts of coated conductors research because most projected applications, both dc and ac, are in magnetic fields. Research is needed on optimizing the flux pinning properties of coated conductors by practical methods. Specific issues include:

- How do intra-grain and inter-grain flux pinning defects affect J_c vs. thickness in coated conductors?
- How do we develop mechanisms and methods to improve intra-grain and inter-grain flux pinning structure?

Breakout Groups 3 & 4: Conductor Design and Engineering

The ultimate architecture of the HTS coated conductor will be determined by various requirements, not all of which are capable of simultaneous optimization. Coated conductors must be protected at local hot spots and for magnet quenches, meaning that both the local YBCO-stabilizer interface resistance and the total parallel conductance of the stabilizer are important. Means to minimize hysteretic losses are important for ac applications and since many of these involve subdivision of the coated conductor, the issue of percolation through the network of barriers within the YBCO is important. For magnet applications the whole angular dependence of the critical current is important because all orientations of the magnetic field with respect to the conductor will occur. Mechanical properties of the conductor are also important, suggesting that architectures that put the YBCO close to the neutral axis are favored. Specific issue include: ac losses; stability; quench protection; conductor geometry; and cost-effective manufacturing. Participants should also considered factors such as tape dimensions, geometry, operating conditions, cost, length of single pieces, amperage, and other electrical, mechanical, and magnetic properties for electric power applications.

The following focus questions were posed within each concurrent breakout group:

- What are the most critical technical developments needed to achieve the conductor envisioned in 2010?
- For the top technical developments, what are their status, targets (2005, 2010), and gaps?
- What R&D activities are needed to achieve the vision?
- For the top R&D activities, what are the interim milestones, performers and linkages?

2.2 Discussion Group I: Substrates/Buffers

Participants: Substrates and Buffers

NAME	ORGANIZATION
Paul Berdahl	Lawrence Berkeley National Laboratory
Claudia Cantoni	Oak Ridge National Laboratory
Najib Cheggour	National Institute of Standards and Technology – Boulder
David Christen*	Oak Ridge National Laboratory
Stephen Dorris	Argonne National Laboratory
Eric Hellstrom	Applied Superconductivity Center University of Wisconsin
Dirk Isfort	Nexans SuperConductors
Dominic Lee	Oak Ridge National Laboratory
Vic Maroni	Argonne National Laboratory
Marshall Reed	U.S. Department of Energy
Kamel Salama	University of Houston
Shara Shoup	MicroCoating Technologies
Xuming Xiong	SuperPower, Incorporated

*** Report Out Presenter**

FACILITATOR: ROSS BRINDLE, ENERGETICS, INCORPORATED

Performance Characteristics

Increasing substrate strength can allow the thickness of the substrate to be decreased and the overall fraction of conductor that is superconductor material to increase, thereby increasing Je. Specific targets included an absolute minimum substrate and buffer strength of 100 MPa, with 200 MPa being more reasonable. In the final HTS coated conductor, achieving 20% of total conductor mass being superconductor is another way to think about this area.

In 2010, substrates will be produced by high-yield processes, possibly through increased width and slitting. In some processes, such as RABiTS, slitting tape could hinder grain size; controlling grain size and grain aspect ratio may help to alleviate these problems and potentially allow higher I_c. Process speed may be more accurately measured in terms of volume per unit time rather than length per unit time. Substrates should be non-magnetic.

There will be a significant effort to reduce the complexity of buffer systems. Buffer systems will be used that provide adequate oxygen and cation diffusion barriers but transmit epitaxy and that can be produced at greater thicknesses without cracking, thereby reducing the number of layers and, consequently, their complexity and cost. Conductive buffer layers, single-layer buffers, or possibly eliminating the need for a buffer layer at all are all advanced concepts that buffer materials may enable.

Consistent, reproducible texture control, to below 5° (possibly 2 °) will be used to achieve the cost points outlined in the vision. At 5°, effects are seen in the buffer and substrate; achieving 2° will allow some flexibility during processing.

By exploring ways to reduce the YBCO synthesis temperature down from 750 C to 600-700 C, greater buffer options may be enabled. Finally, the $1/m of substrate goal that was outlined in the previous roadmap edition remains a valid and worthy goal today.

Summary slide points:

- Consistently produce long lengths (>500 m) of complete substrate with buffer layer with good properties
- Simplify architecture by reducing number of layers (to drive cost down)

- To increase J_e, several options should be explored (double-sided buffers, conductive substrates)
- Substrates should be non-magnetic, preferably conductive
- Bottom line: buffers and substrates are capable of sustaining high J_c

Key Breakthroughs

The breakthroughs that will allow the vision to be realized are grouped into three basic areas:

- Improved Theoretical Understanding
- New Processes For Enhanced Performance
- Scale-Up (Length and Width)

By achieving a more complete basic understanding of texture development and the effect of impurities, granularity, and sulfur superstructure, researchers can more effectively manage substrate textures. Similarly for buffers, understanding how self-planarization and improved texture is achieved by SrRuO3 may lead to new buffers with even better textures. Understanding texturing mechanisms in both substrates and buffers can allow the creation of buffers with sharper texture than substrates. Finally, understanding how texture is affected by specific YBCO processes can lead to greater advances.

Breakthroughs to develop alternative processes that allow for greater process speeds, lower demands on the substrate, improved texture, smaller grains, improved surface finish, and higher yields are central to the vision. Breakthroughs in conductive substrates with high strengths (perhaps copper based) and possibly new geometries (such as round wires) can lead to new systems with improved performance and lower cost. Buffer development may include conducting buffers with low interfacial resistivity, uniform, solution-based single-layer buffers or double-sided buffers, ultimately leading to a "super buffer layer."

The key breakthrough that will allow scale-up of substrate and buffer production to lengths and widths that will achieve the vision cost goals is reliable process control that can sustain properties over long times.

Summary slide points:

- Basic understanding of texture development and effect of impurities
- Understanding of texturing process in relation to geometry
- Process control and feedback over long times
- Conductive buffers with low interfacial resistivity
- Single solution buffer, double-sided, 500A/cm I_c (to increase width)

R&D Activities

The R&D activities needed to achieve the breakthroughs needed for substrates and buffers to ultimately achieve the vision are organized in six general areas:

- Chemical and Physical Characterization
- Mechanical Characterization
- Understanding of Texturing
- Conductive Buffer Layers and Copper Alloy Substrates
- Process Control
- New Concepts

Characterization of substrates, buffers, and entire coated conductor systems will continue to play a central role in the R&D agenda for HTS coated conductors. Developing substrates that are chemically compatible with YBCO and can allow for the elimination of buffer layers can, if technically possible, reduce the overall system complexity and cost. Research on understanding diffusion dynamics through buffers and substrates will aid in materials and system development.

New concepts may offer promise for significant advances in capabilities and/or cost reduction, and R&D that investigates these concepts is crucial. Round wire systems and solution-based deposition techniques are identified as two areas of potential investigation.

Summary slide points:

- Research on diffusion dynamics through buffers and substrates
- Predictive modeling of stress states in the substrate
- Study and modeling of texture in relation to microstructure
- Modeling and experimental studies of deposition and texturing
- Nucleation and growth of "thick" solution buffers with uniform coverage
- Conductive buffers with good diffusion barrier and compatibility with YBCO
- Feedback process control

Take-Home Messages

- Lots of work to do!
- Substrates and buffer layers are the platform to HTS coated conductors – they are critical pieces of the entire CC.
- Process control to obtain length and width is critical to cost-effective manufacture of substrates and buffers.
- Many of the other priorities described are aimed at improving substrate and buffer performance.
- Considering the vision time frame, working with other communities (e.g., process control industry) to accelerate development and scale up may be mandatory.
- Fundamental research and innovation is still strongly needed.

TABLE 2.2.1: CHARACTERISTICS AND FABRICATION OF SUBSTRATES AND BUFFERS IN THE 2010 HTS COATED CONDUCTOR

	PROCESS SPEED	SURFACE FINISH	STRENGTH	MAGNETISM	NEW MATERIALS	OPTIMIZATION	BOTH BUFFERS AND SUBSTRATES *(No Category)*
SUBSTRATES			• Fraction of conductor with supercon-ductor in it should be high (~20%) – Related to strength • Stronger the better to reduce thickness and increase J_e (25 micron thickness)	• Non-magnetic	• Substrate material that meets vision is used (copper?); RABiTS currently too expensive (labor costs) • Aspect ratio of grains can influence I_c – control aspect ratio in 2010	• Thinner, wider substrates for increasing processing yield, lower costs • RABiTS – slitting tape could hinder grain size, in 2010 control grain size better	• Texture control (2^o?); lower affords more margin for error; ~5^o is where effects are seen – Reproducibility • Use homogeneous processes – parameters in substrate and buffer should not vary more than 5% – Reproducibility • Bring YBCO synthesis temperature down (from 750 to 700) to enable other buffer options • $1/m is good substrate cost target • Thermal expansion may be an issue for some materials (e.g., Cu not as close to YBCO) – This is effected by processing, problem in current substrates
SUBSTRATES AND BUFFERS	• ~25 m/n for 10 cm width • Volume/time or volume/ width/time may be more accurate for comparisons across technologies	• Roughness on order of 1 nm. (if buffer can be planarized, can tolerate more roughness) • Closer to 15 nm for ISD	• >100 MPa for substrate and buffer (lower limit, 200 MPa may be more practical)		• Non-reactive to superconductor • Substrate may be used as a stabilizer	• Higher manufacturing yield • Buffer material that is good cation and oxygen barrier but transmits epitaxy	
BUFFERS					• Buffer is simple and thin (least number of layers possible) – Single layer that does it all is ideal • Conductive buffer layer • Interfacial resistivity $<10^{-8}$ Ohm cm^2 • Consider Ni-alloy materials to avoid magnetism,	• Double-sided buffers	

	Process Speed	Surface Finish	Strength	Magnetism	New Materials	Optimization	Both Buffers and Substrates *(No Category)*
					avoid AC loss – Conductivity is high-stability issues • Eliminate buffer entirely • Single layer or functionally graded buffer layer • YBCO on a silver buffer layer • Buffer layer has better texture than substrate • Simplified architecture in buffer layer		

TABLE 2.2.2: R&D NEEDED TO ACHIEVE THE BREAKTHROUGHS AND VISION – SUBSTRATES AND BUFFERS

	NEW CONCEPTS	CHEMICAL/PHYSICAL CHARACTERIZATION	MECHANICAL CHARACTERIZATION	UNDERSTANDING OF TEXTURING	CONDUCTIVE BUFFER LAYERS AND CU ALLOY SUBSTRATE	PROCESS CONTROL
SUBSTRATES		Develop substrates chemically compatible with YBCO so that buffer layers will not be needed ◆◆◆◆	• Predictive modeling of stress-states in the substrate ◆◆◆◆◆ • Mechanical characterization of new substrates ◆	• Study and modeling of texture in relationship to microstructure ◆◆◆◆◆◆ – TEM studies of initial stages of nucleation and secondary recrystallization (substrate) texture		
SUBSTRATES AND BUFFERS	• Round wire ◆◆◆ – Identify filamentary crystal substrates – Buffer and YBCO or – IBAD on round filaments	• Research on diffusion dynamics through buffers and substrates ◆◆◆◆◆◆◆		• Texture maps (EBSP) that distinguish between in-plane and out-of-plane	• Put more effort into new high conducting alloys and buffer deposition on those alloys ◆◆◆ – Rolling/ texturing of Cu alloys	• Feedback process control ◆◆◆◆◆◆◆ – R2R XRO (comparable texture) – R2R IR (comparable strain) – Ellipsometry (thickness) – Build prototype control/monitoring systems (portable) and test at different sites – Define critical process parameters, how to measure them, and how to maintain system in correct window processing all in situ real time – Involve outside

	New Concepts	Chemical/Physical Characterization	Mechanical Characterization	Understanding of Texturing	Conductive Buffer Layers and Cu Alloy Substrate	Process Control
						vendors to "adapt" short length processes to long length – XRO, composition, thickness, etc.
Buffers	• Put more effort into solution-based deposition techniques ◆◆	• Elucidate how buffer layers influence twin structure development in YBCO ◆◆◆ • Doping of buffers to enhance performance • Comparative study of candidate buffer layer materials under "standard" conditions to downselect		• Modeling and experimental study of film deposition and texturing ◆◆◆◆◆ – Study initial stages of formation of buffer on substrate (texturing) – Study buffer texturing in relation to deposition parameters • Nucleation and growth of "thick" solution buffers with uniform coverage ◆◆◆◆◆ – Basic understanding of IBAD MgO and effects of all parameters on texturing and processing windows – Basic understanding of growth evolution of texture in ISD and IBAD – Systematic study of all oxides in relation to ion	• Conductive buffer with good diffusion barrier and good compatibility with YBCO ◆◆◆◆ – Conductive buffers for Cu-based tapes – identify Cu and O diffusion barrier materials, compatible with YBCO deposition – Identify conducting buffers, study changes in electric conductivity, cation/o diffusion and reactivity with YBCO as function of deposition • Doping studies of existing buffers to increase conductivity ◆◆	

	New Concepts	Chemical/Physical Characterization	Mechanical Characterization	Understanding of Texturing	Conductive Buffer Layers and Cu Alloy Substrate	Process Control
				interaction with their crystal structures (IBAD texture) – Systematic study of growth habit of choice • Investigate IBAD/ITEX/ ISD texturing mechanisms ◆◆◆ • Characterize texture development or loss of texture through thickness of buffer layer		

TABLE 2.2.3: KEY BREAKTHROUGHS THAT ENABLED THE VISION TO BE ACHIEVED – SUBSTRATES AND BUFFERS

	BETTER UNDERSTANDING (Theoretical Understanding)	SCALE-UP TO LONG LENGTHS AND WIDTHS (~ 100M; SEVERAL CM)	NEW PROCESSES FOR ENHANCED PERFORMANCE
SUBSTRATES	• Basic understanding of texture development and effect of impurities ◆◆◆◆◆◆ • Understanding of texturing process in relation to granularity ◆◆◆◆◆ • Understanding role of impurities and sulfur superstructure in RABiTS starting material ◆		• Alternative texturing methods that have following advantages ◆◆◆◆ – Fast process speed – Low demands on substrate – Good texture – Small grain – Good surface finish – Simple and high yield • Textured Cu-alloy substrates with high electric conductivity and high strength (≥ 300 MPa) ◆◆◆◆ • New geometry ◆◆◆◆ – Texturing of small round substrates – Round wire-new process • Stronger, thinner metal tapes ◆◆◆ • Substrates with favorable grain aspect ratio ◆ • New metal or alloy which easy to texture and non-reactive to superconductor • Non-metal, high-temperature, flexible, long textured (?) substrates
SUBSTRATES AND BUFFERS		• Process control and feedback over long times ◆◆◆◆◆◆	• Non vacuum-produced substrate/buffer embodiment ◆ • Butt-to-butt conductor geometry for current in and heat out • YBCO deposition at 600-700°C would enable new buffers/substrates
BUFFERS	• Understanding improved texture, self-planarization that is achieved with SrRuO3 → may lead to new buffers with even better texture ◆◆◆ – Understand texture mechanisms in buffer that gives better texturing than substrate – Buffers with sharper texture than substrate – Self-planarizing buffer layers for ISD • Understand buffer/coated conductor reactions for specific buffers with specific YBCO processes ◆◆	• All electrochemical deposition of buffer layer(s)	• Conducting buffers with low interfacial resistivity ◆◆◆◆◆◆◆ • Single solution buffer, double-sided, 500 A/cm = I_c ◆◆◆◆◆ – Uniform solution single buffer • Identify buffer system for Cu-based substrates ◆◆◆ – Buffer on Cu-alloy tapes • Identification of "super" buffer layer does it all ◆◆ • Understand cation and O diffusion and how to limit them ◆ • A buffer/YBCO interface that induces flux pinning in YBCO • IBAD of conductive buffers (on copper) • ISD of conductive buffers • Buffer deposition at 600-700°C

(Comment: to enable critical developments and breakthroughs, a long-range fundamental approach is needed)

TABLE 2.2.4: FIVE MOST WANTED – SUBSTRATES AND BUFFERS

GENERAL COMMENT: Work with communities already working in these areas.

TOP 5 R&D AREAS	KEY TECHNICAL ELEMENTS	ACHIEVEMENT METRIC(S)	YEAR(S) OF ACCOMPLISHMENT (MILESTONES)	RELATED ACTIVITIES – LINKAGES
• Study and modeling of texture in relation to microstructure	• Theory of texture in metals • Deformation parameters which control texturing in metals • Experimental study of effect of microstructure on texturing	• Able to predict texturing (misorientation) parameters in substrate • Ability to control grain size	• <5° 2005 • <2 ° 2008 (consistently)	• Results assist manufacturing of textured metal substrates • Couple heavily with texture community
• Modeling and experimental investigation of film deposition and texturing	• Establish theory • Investigate and improve buffer texturing methods (IBAD, ITEX, ISD, . . .) by experiment, analysis, simulation, and test of models	• Able to predict texturing (misorientation) parameters in buffer	• <5° 2005 • <2 ° 2008 (consistently)	• Results used to improve cost and performance of buffer manufacturing
• Conductive buffers with good diffusion barriers and compatibility with YBCO	• This system would be configured as follows: YBCO, oxygen barrier, cation barrier, and then conductive metal tape • Oxygen barrier layer must have coexistence of electrical conductivity and low O diffusivity. High thermo-dynamical stability • Cation barrier layer must have coexistence of electrical conductivity and low cation diffusivity – N-type oxides?	• Identify conducting oxides compatible with YBCO and with low oxygen diffusivity • Identify cation barrier material with low Cu diffusivity at high temperatures and high electrical conductivity • Optimize: – Structure – Thickness – Deposition parameters – Interfacial resistivity • Demonstrate a stable conductor with J_E = 30-40 kA/cm^2 (side benefit of increased stability)	• Show feasibility by 2005	• Relates to diffusion dynamics • Linked to Cu-alloy tape developments
• Research on diffusion dynamics through buffers and substrate	• Understand effect of buffer crystalline perfection on diffusion coefficient • Study mechanisms of oxygen diffusion through the metal substrate: Does it happen? Is it important • Understand bulk vs. grain-boundary diffusion through functional buffer layers	• Optimize for thinnest and highest-quality architecture (single buffer layer?)	• Basic understanding by 2005 • Optimization by 2007	• Relates to conductive buffer layers

TOP 5 R&D AREAS	KEY TECHNICAL ELEMENTS	ACHIEVEMENT METRIC(S)	YEAR(S) OF ACCOMPLISHMENT (MILESTONES)	RELATED ACTIVITIES – LINKAGES
• Predictive modeling of stress states in all layers	• Define parameters that critically influence stress states of layers of the conductor • Need experimental measures of actual stress states (x-ray, other techniques) • Need relevant materials properties (thermal expansion, Young's modulus, lattice mismatch, others) • Use model to predict effect of various architectures on critical strain of YBCO	• Good agreement between model and experiment for simple system, i.e., substrate/single buffer - 2004 • Build complexity of model to include additional buffers and YBCO – 2005 – Include diffusion characteristics? • Expert system		• Detailed microstructural characterization and determination of growth modes
• Feedback process control	• Thickness (± 10%) • Texture (2° FWHM) • Composition uniformity (± ?%) • Roughness (1nm RMS) • Tools – RHEED, XRD – Ellipsometry – Auger – Optical (visible, IR, UV) – Laser interfermometry	• In-process capability • Feedback/correction • H_2O control • Rastering • Temperature/atmosphere monitoring and control • Target, precursor additive (sulfur)	• 2009	• Linked to YBCO deposition • Measurement criteria and metrics linked to modeling results • This is used ultimately by manufacturers
• Nucleation and growth of "thick" solution buffers with uniform coverage (Note: today, thick (>200 Å) buffers cannot be made without cracking, forcing the use of multiple layers to achieve adequate diffusion barrier, thereby increasing cost)	• Define "thick" – Thick enough to prevent diffusion (~0.5 micron) • Define fracture toughness required to avoid cracking of buffer during drying • Search for additives that increase fracture toughness, reduce shrinkage • Develop, characterize solution chemistry that gives uniform coverage • Need fracture toughness data on buffer/additive systems during drying stage • Early screening step to test many potential materials, narrow down • Ultimately move towards single layers	• Achieve needed thickness without cracks	• Identify good elastome, improve it by 2004 • Single layer – 2006	• Diffusion data or sample tests are used to determine desired thickness • Look to results of some ongoing university projects

TABLE 2.2.5: SUBSTRATES AND BUFFERS – SUMMARY

Performance Characteristics

- Consistently produce long lengths (>500 m) of complete substrate with buffer layer with good properties
- Simplify architecture by reducing number of layers (to drive cost down)
- To increase J_e, several options should be explored (double-sided buffers, conductive substrates)
- Substrates should be non-magnetic, preferably conductive
- Bottom line: buffers and substrates are capable of sustaining high J_c

Key Breakthroughs

- Basic understanding of texture development and effect of impurities
- Understanding of texturing process in relation to geometry
- Process control and feedback over long times
- Conductive buffers with low interfacial resistivity
- Single solution buffer, double-sided, 500A/cm I_c (to increase width)

R&D Activities

- Research on diffusion dynamics through buffers and substrates
- Predictive modeling of stress states in the substrate
- Study and modeling of texture in relation to microstructure
- Modeling and experimental studies of deposition and texturing
- Nucleation and growth of “thick” solution buffers with uniform coverage
- Conductive buffers with good diffusion barrier and compatibility with YBCO
- Feedback process control

Take-Home Messages

- Lots of work to do!
- Substrates and buffer layers are the platform to HTS coated conductors – they are critical pieces of the entire CC.
- Process control to obtain length and width is critical to cost-effective manufacture of substrates and buffers.
- Many of the other priorities described are aimed at improving substrate and buffer performance.
- Considering the vision time frame, working with other communities (e.g., process control industry) to accelerate development and scale up may be mandatory.
- Fundamental research and innovation is still strongly needed.

2.3 Discussion Group 2: RE-123 Nucleation, Growth, and Flux Pinning

By 2010, a fully mature coated conductor product should have the following characteristics: 100 A, 1 cm width, 1 micron film, at 3T and 77 K. A production plant should be able to produce 120 Km/day of this product.

Critical technical breakthroughs in microstructure control, growth and stability, current sharing architecture and geometry, and scale-up are needed to achieve these targets.

Participants: RE-123 Nucleation, Growth, and Flux Pinning

NAME	ORGANIZATION
Paul Barnes	AFRL
Malcolm Beasley	Stanford University
Raghu Bhattacharya	NREL
Lawrence Cook	NIST
Kathleen Dunn	University of Albany
Ron Feenstra	ORNL
Terry Holesinger	LANL
Don Kroeger	ORNL
Don Leibenberg	ORISE
David Larbalestier*	University of Wisconsin
Hee-Gyoun Lee	SuperPower
Beihai Ma	ANL
James Voigt	SNL

*** Report Out Presenter**

FACILITATOR: JOSEPH BADIN, ENERGETICS, INCORPORATED

Research priorities to achieve the 2010 vision include:

- Fast characterization methodology and new instrumentation
- Understanding J_c on all relevant length scales
  - J_c as a function of thickness
- Determine microstructure development at all relevant length scales
  - Systematic microstructural studies, TEM, SEM, etc.
- Process understanding through thermodynamic and kinetic modeling of processing including nucleation kinetics of defects.
- Systematic studies on chemical additions, doping and substitutions and their effects on properties
- Phase diagram studies
- Understanding and measuring AC losses
- Develop template films on round wire/texturing round wire.

These R&D activities will guide texture development in materials and methods to control pinning. In order to advance to large scale manufacturing there needs to be expertise in growing good films fast and in modifying materials to maximize J_c and to simplify fabrication. There needs to be fast, real-time characterization methodologies. In addition, novel approaches that are high-risk, high-payoff need to be pursued.

TABLE 2.3.1: 2010 – CRITICAL TECHNICAL DEVELOPMENTS TO ACHIEVE ENVISIONED CONDUCTORS
(Needed Breakthroughs)

	Microstructure to produce desired properties	RE-123 growth and stability	Architecture Issues	Scale-up Issues
2005	Intrinsic, extrinsic, or both operating for $J_c(d)$ dependence?? Microstructure control at high growth rates.	RE123: ΔT_c = +3 K; Additive pinning; Growth of RE-123 at lower temperatures (< 700˚C)	Development of improved pinning form SC/Cap layers or lattice mismatch; Determine effects of parallel path widths on AC losses	Uniformity of deposition Length, width
2006	Identify pinning defects and determine the elementary pinning force per defect. Elimination of percolation due to grain boundaries.	Understand origin of flux pinning Rapid oxygenation process for all processes.	Development of simplified buffer layer architecture. Current sharing architextures (e.g.) double side tapes, conductive buffers.	Determine limit of growth rate / throughput
2007	Devise processing route to achieve high density of the pinning defects (with no degradation of J_c)	Reproducible control of liquid to maximize growth rate and optimize microstructures	Reduce grain size in RABiTS to < 5μm.	Incorporation of flux pinning technologies
2008				YBCO filamentation – AC losses
2009	A route to achieve alignment of round wires, etc?			High growth rate and throughput
2010			Round wire architecture	Round wire technology.

TABLE 2.3.2: R&D ACTIVITIES TO ACHIEVE 2010 VISION
(RAW LIST)

1. Systematic studies of chemical addition / substitution for better performance.
2. Purity of precursors / starting materials.
3. Comprehensive study of cost vs. performance.
4. Develop deposition / processing technology for round wire technology
5. Fast characterization; methodology and new instruments
6. Correlation of length scales with properties (Microstructural vs. mesoscopic)
7. Processes for insertion of flux pinning structures
8. In-situ characterization for process modeling during growth
9. Kinetics of crystallographic defect formation
10. Measurement of Jc of individual grain boundaries to determine effects of types of misorientation
11. Study mechanisms of defect generation and defect formation and microstructure evolution (TEM and modeling)
12. Systematic Microstructural studies TEM, SEM, etc.
13. Thermodynamic and kinetic modeling of processing, nucleation and kinetics
14. Jc –thickness (film thickness and through-thickness film Jc)
15. RE substitution
16. Determine liquid phase field for selected systems
17. Study effect of growth rate on Jc / defect formation
18. Control studies to introduce specific defect types (effect on Jc(H,Ø,T)
19. Understand phase stability under relevant processing conditions.
20. RE solid solubility as f(P(O2), T)
21. Fundamental limits on strength of flux pinning in RE-123
22. Develop method to produce and control property – flux pinning and rapid oxygenation.
23. Develop instrumentation to support on-line Ic measurements.
24. Improve modeling of real tape/wire stability/dc/ac losses
25. Broaden deposition window T, P(O2)
26. Grain boundary understanding at atomic level.
27. Develop compositional and processing for small grains in textured metals.
28. Measure AC losses in striated YBCO conductors.
29. AC losses.

TABLE 2.3.3: R&D ACTIVITIES TO ACHIEVE 2010 VISION
(SORTED LIST)

Characterization
1. Fast characterization – methodology and new instrumentation (6 votes)
2. Process control tools (1 votes)
3. Develop instrumentation support for on-line Jc measurement (quality control)
4. Incorporate characterization for process monitoring during growth – XRD, Raman, Auger, etc. (4 votes)

Understand J_c on All Relevant Length Scales
1. Measure Jc of grain boundaries to determine effects of types of misorientations. (1 vote)
2. Jc as a function of thickness (8 votes)
   a. Variable thickness of films.
   b. Through thickness of the film
3. Effect of growth rate on Jc / defect formation (4 votes)
4. Develop processes to install flux pinning defects (8 votes)
5. Control studies to introduce specific defect types; effect of Jc(H,Ø,T) (2 votes)
6. What are the fundamental limits on strength of flux pinning in RE-123 – What is max Jc(B)? (4 votes)

Determine Microstructure Development at All Relevant Length Scales
1. Correlation of length scales (defect) with properties – mesoscopic and microscopic. (2 votes)
2. Build understanding of G.B.'s at atomic level.
3. Systematic Microstructural studies TEM, SEM, etc. (7 votes)
4. Study of mechanisms of defect formation and microstructure evolution (TEM and modeling)

Process Understanding (modeling)
1. Thermodynamic and kinetic modeling of processing including nucleation kinetics of defects, etc. (6 votes)
2. Broaden deposition window (T, P(O2),…)
3. Determine liquid phase field for selected systems (1 vote)
4. Develop method to produce and control –support flux pinning investigations and rapid oxygenation.
5. Develop low cost precursors (Ic as a function of materials cost, purity) (2 votes)
6. Growth rate experiments – characterization (1 vote)
7. Cation diffusion issues: time, temperature, barrier layers, etcs. (1 vote)

Chemical Substitutions, Doping, and Other RE Systems
1. Systematic studies on chemical additions, doping, and substitutions – effects on properties. (4 votes)
2. Kinetics of crystallographic RE defect formation
3. Understanding phase stability under relevant processing conditions.
4. RE solid state solubility as a F(T, P(O2))
5. Phase diagram study – (4 votes)
   a. low P(O2) pressure
   b. role of fluorine
   c. RE substitution
6. RE substitution-effects in presence of liquid phases.

Stability and AC Losses

1. Measure AC losses in stirrated YBCO films.
2. AC losses (3 votes)

a. Grain size
b. YBCO growth in filaments
c. Current sharing
d. Tradeoff of modeling twists, filaments, etc.

3. Improved modeling of real tape/wire stability/quench/DC AC loss / architecture – theoretical modeling needed.
4. Develop metal compositions and processing for small grains in textured metals

Technical Issues

1. Develop deposition / processing technology for round wire technology
2. Template films on round wire/ texturing round wires (3 votes)
3. Characterized ≈ 5cm wide MOCVD / MOD samples vs. processing parameters (1 vote)
4. HTS film thickness vs strain tolerance (2 votes)
5. Develop process understanding (technical issues)
6. Comprehensive study of cost vs. performance

TABLE 2.3.4: TOP 5 HIGHEST RATED R&D ACTIVITIES TO ACHIEVE 2010 VISION.

R&D Activity	Technical Elements	Achievement Metric	Year of Accomplishment (2005-2010)	Related Activities / Linkages
Understanding J_c on all relevant length scales	(1) pinning identify key pin types density, strength, causes (2) Jc vs thickness – identify material dependent contributions to Jc(t) – obtain material independent Jc(t) (3) GB'S understand Jc (Ø,H,T, facet plane) – guide to texture and process development (4) find ways to amerliorate GB effects e.g. doping	(1) CC Angular anisotropy better than BSCCO conductors 30 K (2) Understand cross-over from pinning to weak links (3) Understand flaw characteristic determine significance for Jc (4) flat GB Jc dependence out to 10˚ 77K	(1) 2005 (2) 2006 (3) 2006 (4) 2007	Guide texture development in materials and buffers. Process understanding to install pins.
Processing Understanding (How to grow films fast)	(1) Structural and phase characterization (including liquid phases) (2)Increase process rate and related property dependence (3) Liquid phase field for selected systems (4) Thermodynamic and Kinetic modeling (5) Phase diagrams-thermo and kinetic data for modified materials	Processing method capable of 1000 A/cm-width (2) enhanced flux pinning (3) high rate production	1000 A/cm-width SF (2005) 1000 A/cm-width 3T (2010) flux pinning enhancement (2007) 120 km/day / plant (2008)	Understanding Jc Modified materials Large scale manufacturing
Modify Materials to Maximize J_c, simplify fabrication	(1) Phase equilibria and stability of RE123 mixed systems (2) Pinning topology – understanding modeling Comparison of	Higher T_c and J_c 1000 A, 3T, 77K, 1 µm x 1 cm		Process understanding Microstructural studies Jc understanding on all scales

R&D Activity	Technical Elements	Achievement Metric	Year of Accomplishment (2005-2010)	Related Activities / Linkages
	methods (3) Introduction of flux pinning centers – processing, chemical subs, physical subs, porosity, interfacial (4) Comparison of mixed RE-123 systems.			
Develop fast characterization methodologies	(1) Defect Correlation database TEM,SEM (2) In-situ diagnostics (RHEED, RAMAN, XRD, Ion scattering, AA) (3) Rapid defect detection	(1) Database development and dissemination (2) Demonstrated real-time process feedback (3) Demonstrated fast post-mortem defect detection	2005 - Database started 2005 – real time process via in-situ probe 2007 – demonstration on pilot line 2007 – defect identification over 100m piece length < 5 min	Jc understanding Process development Material modification Large scale manufacturing
Novel Approaches (High risk / high payoff)	(1) Round wires – deposition process Templates and substrates (2) Less anisotropic superconductor	J_c > 1 MA/cm^2 at H=0 theshold of interest δ < 5	2005	Substrates Growth mechanisms

RE 123 Nucleation, Growth and Flux Pinning

Vision 2010

➔ **Vision**

- **Low cost, High Performance HTS CC's**
  - a. Available 2005
  - b. 100 m lengths
- **LN_2 Applications**
  - a. < $50/kA-m by 2005
  - b. 20-60K; < $30/kA-m by 2005
- **2010: Price performance**
  - a. Improvement by factor of 5 for km lengths over 2005 price levels.

Targets 2010

- Fully Mature Technology
  - ✓ 1000 A / 1 cm width / 1 μm film / 3 T, 77K
- Processing rate: 120 km / day /production plant (scalable equivalent)
- Deposition control
  - ✓ Uniformity / reproducibility
  - ✓ < 5% end-to-end variation (100+ lengths)
- Materials improvement
  - ✓ T_c raised 5-10K RE123 system
  - ✓ Flux pinning Hirr (77K) ≥ 10 T
- Conductor performance
  - ✓ $I_c(H||ab) / I_c(H(45^\circ)) < 2$
  - ✓ Reduced aspect ratio (round, square wire???)

Critical Technological Developments Needed

- Optimal microstructure to produce desired properties
- Growth processes and process stability
- Architectural issues
- Scale-up issues

Research and Development Areas

- Characterization tools
- Understanding J_c on all relevant length scales
- Determine microstructure development on all relevant length scales
- Process understanding (modeling)
- Chemical substitution and other RE-123 systems
- Stability and AC losses
- Technical issues -

Priority R&D Activities

- Understanding J_c on all relevant length scales
  - ✓ Manufacturing defects
  - ✓ Intermediate scales - Jc versus thickness
  - ✓ Microscopic - flux pinning defects (what are they??)
- Process Understanding (how to grow good films - fasssst)
- Modify materials to maximize J_c, simplify fabrication
- Develop fast characterization methodologies
  - ✓ Data base correlations between “slow” characterization and “fast”
  - ✓ In-situ and post mortem
- Novel approaches (high risk, high payoff)

2.4 Discussion Group 3: Conductor Design and Engineering A

Conductor Design & Engineering A

For applications in liquid nitrogen, the wire price should be less than $50/kA-m in 2007 (not 2005). By 2010, it should be $10/kA-m. The Vision should be changed to reflect this estimate. The ability to achieve these goals depends on the availability of Title-3 funding and SPI material requirements.

The geometry for conductors must be identified as soon as possible to serve as research targets. The recommended basic building block design for power applications in 2010 is:

Particpants: Conductor Design & Engineering A

NAME	ORGANIZATION
Jack Ekin	National Institute of Standards and Technology, Boulder
Brady Gibbons	Los Alamos National Laboratory
Alex Ignatiev*	University of Houston
Bob Lawrence	BL&A, Incorporated
David Lindsay	Southwire Company
Chuck Oberly	AFRL
M. Paranthaman	Oak Ridge National Laboratory
Dean Peterson	Los Alamos National Laboratory
John Scudiere*	American Superconductor Corporation
Masaki Suenaga	Brookhaven National Laboratory
Yi-Yuan Xie	SuperPower Incorporated

*** Report Out Presenters**

FACILITATOR: MELISSA EICHNER, ENERGETICS, INCORPORATED

- Face-to-face
- Neutral axis
- Alternate conductor designs; Conducting substrate
- 2-sided coating
- Current carrying capacity of stabilizer
- Low ac loss; geometry; multi-filamentary
- Filament size > 10 μm
- Substrate thickness; 25-50 μm
- Multi-layer for ac loss
- Piece length 1000 m
- Physical size < 1 cm for width

In 2010, the recommended performance and operating specifications are:

- J_E 30-65 K; 3 T; 10,000 – 20,000 A/cm^2
- Stabilizer design
- 200 MPa stress (300 MPa) @ 77 K
- Irreversible strain limit 0.6 % tension; 1% compression (for magnets)
- 2 cm bend diameter
- n value ≥ 14
- 1000 A/cm-width; I_c 77 K; sf
- 100-200 A @ operating conditions
- J_E 10,000 – 20,000 A/cm^2 @ operating conditions

In addition in 2010, scale-up and cost-effective manufacturing targets, as well as integration/engineered conductor targets, should be:

- Wide width 10 cm
- 10,000 km/year and $10/kA-m
- Minimum 3 U.S. wire manufacturers
- Non-resistant joint (superconducting)
- 100 thermal cycles survivability
- Coils 1000 load cycles

Research priorities to achieve the targets include:

- Develop soldering and connecting technologies to optimize both sides (i.e., no bad side)
- Analysis and modeling of tradeoffs of stability, quench protection, and AC losses for specific applications
- Ensure uniformity of 10,000 km, 10cm, and 2 μm
- Process improvements and cost reduction

To achieve the targets by 2010, the process must be identified as soon as possible so demonstrations can start in 2006. The specifications are expected to progress over time and the improvements must be tested to assure that they are meaningful to customers.

TABLE 2.4.1: 2010 CONFIGURATION
DESCRIBE CHARACTERISTICS AND FABRICATION OF THE HTS CONDUCTOR PRODUCT THAT ACHIEVES THE VISION

	CRITICAL BREAKTHROUGHS REQUIRED (FY04-FY09)	CHARACTERISTICS OF HTS CONDUCTOR IN 2010
BASIC BUILDING BLOCK DESIGN FOR POWER APPLICATIONS (CONDUCTOR GEOMETRY)	• 2004 - Coil and wire manufacturers working together • 2004 - Test systems for filaments, HTS, multilayer, neutral axis, stabilizer • 2004 for 2007 - Pilot facility with new equipment operating 1,000 km	• Conducting substrate • Conducting buffer layer • Face to face • Neutral axis • Low AC loss geometry (multi-filamentary) • Substrate 25-50 μ thick • Piece length 1000 m • Current carrying capacity of stabilizer • 2-sided coating • Filament size >10 μ • Multi-layer for low AC loss • Physical size <1 cm for width
PERFORMANCE AND OPERATING SPECS	• 2004 (FY05) – 250 A/cm width 20 m • 2005 (FY06) – 300 A/cm width 20 m • Flux pinning improved 2-3T • 2005 - Study and make recommendations for AC loss, quench protection, stability • 2006 (FY07) – 350 A/cm width 100 m • 2007 (FY08) – 400 A/cm width 1000 m • 2007 – Standards upgraded to match real applications I_c definition: 1μ v/cm • 2008 (FY09) – 450 A/cm width 1000 m	• J_e 30-65; 3T 10,000 – 20,000 A/cm^2 • Stabilizer design • Irreversible strain limit 0.6% tension 1% compression (magnetic) • N value $\geq$14 • 100-200 A at operating conditions • 200 MPa stress (300 MPa) at 77K • 2 cm bend diameter • 1000 A/cm width I_c 77K sf • J_e 10,000 – 20,000 in operating condition
SCALE-UP AND COST-EFFECTIVE MANUFACTURING	• 2004 – Sliting, lamination demo in – tested • 2004 – Demo 4 cm wide manufact (250 A/cm) all steps • 2005 – Continuous process to produce 2-sided coating by • 2006 – Long length continuous pattering– validate need • 2007 – 200-1000 km available for SPI applications • 2007 – $50/kAm • 2004 for 2007 – Pilot facility, demo width, handling equipment • 2008 – SPI 1000 km • 2009 – SPI 2000 km	• Target • Wide width 10 cm • 10,000 km $10/kA-m • Min 3 U.S. manufacturers

	Critical Breakthroughs Required (FY04-FY09)	Characteristics of HTS Conductor in 2010
Integration Issues of Engineered Conductors	• 2004 – Joining demo (resistant) • 2004 – Customers test joints • 2004 – Insulation with cryogenics and low partial discharge capability, 60-300K • 2005 – Vacuum integrity • 2004-2006 – Coil and wire integration (system design) • 2004-2006 – Cable and wire integration (system design) • 2006 – Insulation vacuum compat. pliable, high break down voltage 60-300k • 2007-2008 – Refrigeration available 5 kW at 77K 200-300 W at 35-40K • 2008 – Superconducting joint demo	• Non-resistant joint (superconducting) • 100 thermal cycles survivability • Coils – 1000 load cycles

TABLE 2.2.4: R&D ACTIVITIES TO ACHIEVE THE VISION

MATERIALS	EQUIPMENT AND PROCESSING	CHARACTERIZATION	PERFORMANCE	APPLICATIONS SUPPORT
• Single buffer/simplified buffer (mod – thin – fewer) ◆◆◆◆◆◆ • All MOCVD processing ◆◆◆◆ • Conducting substrate and buffer ◆◆◆ • Optimize J_c (77K) versus film thickness in long lengths ◆◆ • All MOD process (buffers and HTS) ◆◆ • Development of smaller grain size templates (buffer/substrate) ~10μm size ◆◆ • Explore "alternate conductor designs" to neutral and face-to-face ◆ • New IBAD templates (simple conducting) ◆	• Moving to 10 cm and 25 μm ◆◆◆◆ – Tape handling – Ensuring continuity • In-situ quality control ◆◆◆ • Lower cost manufacturing process development ◆◆ • Process throughput improvement ◆ • Pilot plant equipment and commissioning ◆ • HTS dep. rate - increasing	• AC loss #'s vs. configuration and stability and quench protection (analysis and modeling of tradeoffs of stability, quench protection and ac loss for specific applications) ◆◆◆◆◆◆◆◆◆◆◆◆ • Soldering/connecting no "good side" vs. "bad side" ◆◆◆◆◆ • Mechanical testing: $\in_{irr}$ of new geometries/mat. Slitting – fatigue tests joint tensile strength high field electro-mech ◆◆◆ • Establishment of accelerated testing of HTS cables	• Double today's J_c via flux pinning ◆◆◆ • Methods of utilizing the angular dependence ◆◆ • Uniformity study and optimization across width as well as length for web-coating Testing on wide tape ◆◆ • Consistent properties with length ◆ • Specify stabilizer current carrying capability based on J_e, practical application: cable, magnet	• Coil development ◆◆◆◆ • Pulse tubes 1 kW @ 77K ◆◆ • Cryogenics, dielectrics and insulation ◆◆ • Cable development ◆

TABLE 2.4.3: ANALYSIS OF TOP 4 R&D ACTIVITIES

TOP 4 PRIORITIES	YEAR OF ACCOMPLISHMENT (2005-2010)	ACHIEVEMENT METRIC (characteristic when successful)	RELATED ACTIVITIES/ LINKAGES	TECHNICAL ELEMENTS (DETAIL)
AC losses values vs. configuration and quench protection – analysis and modeling of tradeoffs of stability, quench protection and AC losses for *specific applications*	• 2007	• 20 kJ magnet successfully and repeatedly quenched • Critical path – show stopper	• 2004 – Slitting, grain size, patterned and geometry of conductor • Coil development	• 2005 – Test coil AC losses configuration • 2004 – Test wire AC losses configuration • 2005-2006 – Test stability and quench protection of the coil • 2005 – Implement successful AC wire strategy – make narrow tape filamentized, patterned
Process improvement and cost reduction	• On-going – targeted to meeting 2010 goal	• 2010 –$10/kA-m • 2007 – $50/kA-m	• Mechanical testing ongoing as new material is developed Ongoing 2010 • Improve substrates (non magnetic) – on-going • 2005 – Yield, quality control (in situ monitoring) • 2006 – I_C testing (non-contact) • 2006 – Measurement standards I_C, AC loss • Cost analysis – ongoing	• 2006 – Single buffer and simplified buffer (mod, thin, fewer) cost reduction • 2006 – All MOCVD processing – cost reduction • 2006 – All MOD process • I_c improvement in field 2-3T 30-65 K – 2006 – Characterization – 2010 – Implementation • 2006 – YBCO J_c improvement with thickness
Soldering/Connecting no "good side" vs. "bad side"	• 2008	• 2005 – Effective resistive joint • 2008 – Superconducting joint	• 2006 – Conducting buffer and substrate	• $10^{-9}\Omega - cm^2$
Moving to 10,000 km in 2010, 10 cm and 25 μm – Tape handling – Ensuring continuity	• 2010	• Capacity for 10,000 km/yr for SPI and DOD applications	• 2007 – Dielectrics • 2008 – Refrigeration • Ongoing – Cable development • 2005 – Textured substrates at full scale production • Ongoing – Track international success • Ongoing – Validation of cost models • Ongoing – ≥3 U.S. manufacturers (wire) • 2005-Ongoing – Develop SPI demonstrations and facilitate commercial pull • 2005 – Slitting and lamination • 2006 – Insulation and joints	• 2004 – Funding in place for pilot • 2007 – Pilot facility operation with 1000 km capability per year 1 km piece length • Stage gates • 2004 – 4 cm process operational • 2004 – Demo 10 cm critical path steps • 2004 – Companies must select process

Conductor Design & Engineering A
Vision

- **Group recommended to change the Vision from 2005 to 2007 to achieve $ 50/kA-m**
  - **Depends on Title-3 funding & SPI material requirements**
- **By 2010; $ 10/kA-m; 10,000 km/year**

Target (2010)
Critical breakthroughs required

- **Basic building block design for power applications – conductor geometry**
  - **Face to face**
  - **Neutral axis**
  - **Alternate conductor designs; Conducting substrate**
  - **2-sided coating**
  - **Current carrying capacity of stabilizer**
  - **Low ac loss; geometry; multi-filamentary**
  - **Filament size > 10 μm**
  - **Substrate thickness; 25-50 μm**
  - **Multi-layer for ac loss**
  - **Piece length 1000 m**
  - **Physical size < 1 cm for width**

Target (2010)

- **Performance & Operating specs**
  - **J_E 30-65 K; 3 T; 10,000 – 20,000 A/cm^2**
  - **Stabilizer design**
  - **200 MPa stress (300 MPa) @ 77 K**
  - **Irreversible strain limit 0.6 % tension; 1% compression (for magnets)**
  - **2 cm bend diameter**
  - **n value ≥ 14**
  - **1000 A/cm-width; Ic 77 K; sf**
  - **100-200 A @ operating conditions**
  - **J_E 10,000 – 20,000 A/cm^2 @ operating conditions**

Target (2010)

- **Scale-up & Cost-effective manufacturing**
  - **Wide width 10 cm**
  - **10,000 km/year; $ 10/kA-m**
  - **Minimum 3 U.S. wire manufacturers**

Target (2010)

- **Integration; Issues of Engineered Conductors**
  - **Non-resistant joint (superconducting)**
  - **100 thermal cycles survivalability**
  - **Coils 1000 load cycles**

Conductor Design & Engineering #1
R & D Activities to achieve the Vision

- **Materials**
- **Equipment & Processing**
- **Characterization**
- **Performance**
- **Applications Support**

Top 4 R & D activities

- **A.C. losses # s-vs. – configuration & quench protection – Analysis & modeling of trade offs of stability, quench protection and AC losses for specific applications**
- **Process Improvement & Cost Reduction**
- **Soldering/Connecting**
- **Moving to 10,000 km in 2010**
  Moving to 10 cm and 25 μm – tape handling; ensuring continuity(uniformity) 10,000 km

A.C. losses # s-vs. – configuration & quench protection – Analysis & modeling of trade offs of stability, quench protection and AC losses for specific applications

- **Year of Accomplishment (2005-2010)**
  - **2007**
- **Achievement Metric (characteristic when successful)**
  - **Critical path – show stopper**
- **Related Activities/Linkages**
  - **Coil development**
  - **Slitting, grain size patterned & geometry of conductor (2007)**
- **Technical Elements (detail)**
  - **Test wire; a.c. losses, configuration (2004)**
  - **Test coil/a.c. losses configuration (2005)**
  - **Test stability & quench protection of the coil (2005-2006)**
  - **Implement successful ac wire strategy in 2005; make narrow tape, filamentized, patterned**

Process Improvement & Cost Reduction

- Year of Accomplishment (2005-2010)
  - On-going; targeted to meeting 2010 goal
- Achievement Metric (characteristic when successful)
  - $ 50/kA-m by 2007
  - $ 10/kA-m by 2010
- Related Activities/Linkages
  - Yield quality control 2005 (in-situ monitoring)
  - Ic testing (non-contact) 2006
  - Measurement standards (Ic, a.c. loss)
  - Cost analysis (on-going)
  - Mechanical testing (on-going as new material arrives; 2010
  - Improve substrates (non-magnetic) on-going
- Technical Elements (detail) (cost reduction)
  - Single buffer & Simplified buffer (MOD, thin, fewer) 2006
  - All MOCVD processing 2006
  - All MOD process 2006
  - YBCO Jc improvement with thickness 2006
  - Ic improvement; in-field 2-3 T; 30-65 K
    - Characterization 2006; implementation 2010

Soldering/Connecting

- Year of Accomplishment (2005-2010)
  - 2008
- Achievement Metric (characteristic when successful)
  - Effective resistive joint 2005
  - Superconducting joint 2008
- Related Activities/Linkages
  - Conducting buffer & substrates 2006
  - Dielectrics 2007
- Technical Elements (detail)
  - 10^{-9} Ω.cm^2

Moving to 10,000 km in 2010
Moving to 10 cm and 25 μm – tape handling; ensuring continuity(uniformity) 10,000 km

- **Year of Accomplishment (2005-2010)**
  - **2010**
- **Achievement Metric (characteristic when successful)**
  - **Capacity for 10,000 km/year for SPI & DOD applications**
- **Related Activities/Linkages**
  - **Refrigeration 2008**
  - **Tract international success; on-going**
  - **Develop SPI demonstrations & facilitate commercial pull 2005-on-going**
  - **Cable development; on-going**
  - **Validation of cost models; on-going**
  - **Slitting & lamination 2005**
  - **Textured substrates at full scale production 2005**
  - **≥ 3 U.S. manufacturers (wire); on-going**
  - **Insulation & joints 2006**
- **Technical Elements (detail)**
  - **Stage gates – 4 cm process operational in 2004; funding in place for pilot in 2004; demo 10 cm critical path steps 2004; companies must select process in 2004**
  - **Pilot facility operation w/ 1000 km/year capability by 2007 in 1 km piece length**

2.5 Discussion Group 4: Conductor Design and Engineering B

Summary

The design and engineering of the coated conductor will integrate the sub-parts/layers of the conductor into a cost-effective, robust electric transmission device. Critical developments from now to 2010 in the areas of: conductor geometry, performance and operation, and manufacturing will help achieve the vision of the future.

By 2010, filaments satisfy the stability criteria to withstand 10 times more fault current than required by conventional equipment. AC losses, possibly one the biggest challenges for coated conductors, will be 0.25 W/kA-m. In addition to meeting all performance and design targets, coated conductors will be manufactured for less than $10/kA-m and be capable of 100 meters per hour processing rate.

To reach the 2010 targets, there will need to be critical technical developments in basic building block design, performance, and manufacturing. Practical superconducting joints and field splices will be developed by 2005. By 2007, technical breakthroughs in flux pinning will improve the operation of the coated conductor. AC losses will be low over long conductor lengths in 2007, due to filamentary technical advancements.

Research and development is needed to investigate the basic technology, structure and manufacturing of coated conductors. Activities to characterize the performance and operation are needed, as well as activities to develop tools for modeling and measuring. The top five R&D activities needed to reach the goals and ultimately the vision of 2010 are:

- Understand the process, property and structure of Jc (B, θ, T)
- Develop a method of making and transposing filaments
- Design and test prototype CC's under the device conditions
- Scale-up manufacturing process rates and throughputs
- Understand quench through modeling and measuring the stability and thermal protection

The work breakdown structure of the top five R&D activities can be seen in Table 2.5.4.

It is important to recognize that there is a broad range of activities that need to be completed, in addition to the top five R&D activities, to achieve the coated conductor of the future. Many of these activities are intertwined with each other and the success of one activity can affect the outcome or desired result of another activity (positively or negatively). The impact of these activities will greatly depend on the interaction

Participants: Conductor Design and Engineering B

NAME	ORGANIZATION
Les Fritzmeier*	MetOx
Don Glenn	BL&A
Bob Hawsey	Oak Ridge National Laboratory
Ken Marken	Oxford Instruments
Venkat Selvamanickan	SuperPower
Steve Umans	Rockwell/ MIT
Phil Winkler	Air Products and Chemicals, Inc
Alan Wolsky	Argonne National Laboratory

*** Report Out Presenter**

FACILITATOR: DAN BREWER, ENERGETICS, INCORPORATED

between the users and manufacturers of coated conductors. It is important that they communicate with each other on the technical specifications and capabilities of the coated conductor product. Finally, a DOE supported and coordinated public/private activity in the design and engineering of coated conductors will provide the resources for organizations to successfully achieve the vision. DOE has unique technical capabilities and experience to facilitate a "Conductor Design and Engineering Initiative" (CDEI).

TABLE 2.5.1: 2010 TARGETS

BUILDING BLOCK DESIGN- CONDUCTOR GEOMETRY	PERFORMANCE AND OPERATION	SCALE-UP AND COST-EFFECTIVE MANUFACTURING
• Filaments with size that satisfies needed stability criteria • Quasi-round- able to twist and transpose • Splicing technologies for multi-layered, dissimilar electric functions • 50 nano-ohms cable • Two conducting sides directly connected to superconductor sides • 0.4% Critical strain • Dielectric coating for all applications • Dielectric integration and conductor geometry for high voltage (138 kV)	• Stability- Withstand 10x fault current for longer than required by conventional equipment • Quench robustness and detection • Withstand thermal cycles without tape degradation (under pressurize liquid nitrogen) • Fatigue requirements • 1000 Thermal cycles • Critical stress= 300 MPa under operating conditions • Science Magnetic Field Applications- persistent current, n>30 that enables NMR insert • Power Magnetic Field applications for DC- J_e= 2 x 10^8 A/ m^2 at 4 T • J_e > 10^4 A/cm^2 at 3T and 65 K • 100 A at 4 mm and 1 T • AC losses of 0.25 W/kA-m when would in coil or cable (achievement depends on tape and winding)	• < $10 / kA-m • 100 m/h processing rate • 300 A at 4 mm for $10 /kA-m

TABLE 2.5.2: NEEDED BREAKTHROUGHS

BASIC BUILDING BLOCK DESIGN	PERFORMANCE AND OPERATION	SCALE-UP AND COST EFFECTIVE MANUFACTURING
• Superconducting joints and field splices (2005) • Complete template (ready for HTS) < 25 microns thick (2005) • Dielectric material for cryogenic high voltage applications (2007)	• Magnet and coil stability and quench protection prototypes (2005) • Enough copper for stability, but not too much to decrease J_e (2005) • Flux pinning and/or improved J_c (2007) • Filamentary conductor that leads to low AC loss and current sharing over long lengths (2007) • Develop low aspect ratio for conductor template (2007)	• Modular design for capital equipment (2005) • Slitting technology with <5% reduction in I_c (2005) • Uniform I_c over wide substrates (2006) • Smaller minimum economic plant size (2007) • Reliability demonstrations in devices with second generation (2008)

TABLE 2.5.3: R&D ACTIVITIES

STRUCTURE	CHARACTERIZATION	MANUFACTURING	TOOLS	BASIC TECHNOLOGY
• Develop methods of making and transposing filaments – Cut CC into thin filaments – Coat with resistive copper jacket – Twist into conductor ◆◆◆◆◆ • Develop quasi-round textured template – Develop process for low aspect ratio conductor (epitaxial J_c required for high value AC) ◆◆ • Develop persistent joints • Develop copper alloy with single buffer layer and YBCO in 1 km lengths	• Design tests of prototype CC's • Aging • Thermal cycling • Mechanical environment (handling, winding, etc) ◆◆◆◆◆ • Develop measurements of stability and thermal protection ◆◆◆ • Characterize mechanical fatigue ◆ • Explore magneto-optic imaging of AC in CC ◆	• Develop process design engineering to scale up processing rates and throughputs – Evaluate cost vs. performance trade-offs – Quality control ◆◆◆◆◆ • Develop splice configuration for – Ease of execution – Electrical integrity – Flexible application (Cable fabrication, machine windings) – Effective terminations where current can be injected into all CC layers/filaments – Technology for adjoining 2G conductors ◆◆◆ • In-line process control for all steps ◆ • Single buffer layer at high rate ◆ • Slit wide tapes to get uniform I_c in all tapes ◆ • Repair damage and defects in all process steps • Increase deposition rate of HTS layer by 5x	• Develop device specifications master list (and conductor properties) ◆ • Extend statistical modeling from substrate to complete conductor ◆ • Develop engineering models Stability Thermal protection • Develop quick and effective means of measuring current distribution along width and length	• Understand process/properties/structure of J_c (B, θ, T) – Improve extrinsic pinning to achieve 100 A at 77 K, 1 T in 4 mm widths – Enhance Ic by 3-5 x at 50-60 K through materials modification ◆◆◆◆◆◆ • Improve understanding of quench in engineering application that lead to improved conductor design and improve equipment design ◆◆◆◆◆ • Develop serious computer modeling of AC current and thermal transients – Construct conductor with a variety of copper stabilizers, measure thermal, thickness, and alloys ◆◆ • Develop dielectric material for cryogenic high voltage applications "individual tape" ◆◆ • Understand substrate issues and limiting texture ◆ • Improve conductor yield stress and modulus ◆ • Research current shunting to both sides of the HTS layer ◆ • Develop higher J_c in films 1-3 microns ◆ • Identify and eliminate substrate defects

TABLE 2.5.4: PATHS FORWARD

TOP R&D ACTIVITY	TECHNICAL ELEMENTS	ACHIEVEMENT METRIC	YEAR OF ACCOMPLISHMENT	RELATED ACTIVITIES/LINKAGES
Develop a method of making and transposing filaments	• Investigate CC geometry in relation to AC losses • Subdivide wide filaments • Substrates with fine grains • Testing filamentary conductor • Deposit selectivity on current process • Resistive jacket • Non-destructive to process	• 25 W/ kA-M at 77 K • Develop low AC loss 2G conductor (100-m) suitable for prototype cables and transformers (2007)	• 2010 • Testing completed in 2008	• Modeling AC losses • Cryostabilization • Pre-commercial lengths (10-100 m) of quasi-round "3G" wire demonstration
Design and test prototype coated conductor's under device conditions-aging, thermal cycles/shocks and mechanical environment (handling, winding)	• Small-scale device • Determine critical prototype testing condition for feedback in architecture and design	• 1 m prototype conductor tested • Small coil form • Repeat if prototypes cannot meet requirements (low AC loss, high field conductor)	• 2005 • 2008- Develop in-depth understanding of current flow and limitations of basic and advanced conductor geometries	• Outputs can be used for models • Feeds into conductor design • Predictive models and properties of 2G components for "expert systems" to produce conductor "building block" designs
Understand process/ property/ structure of J_c (B, θ, T)	• Fundamental characterization and structure properties • Testing at different field loading, compare performance of conductors by different HTS process	• Achieve 100 A at 77 K, 1T in 4 mm widths in minimum I_c orientation • J_e> 10^4 A/cm2 (3T, 65K)	• 2008 • 2010	• Evaluate alternative RE-123 compositions for optimum J_c (B, θ,T)
Develop process design engineering to scale up processing rates and throughputs	• Understanding upper limits of process (liquid) • Increase width of material • Understand variability within process area	• Throughput processing @ 100 m/h linear speed at full width • < $10 kA/m – including stabilization and termination • 20 m/h	• 2010 • 2010 • 2005	• Real-time processing monitor and control • Single/thin buffer layer (increasing Ic at given thickness)
Understand quench in engineering activities	• Measurements of stability and thermal protection • Modeling		• 2005	• Develop application models • Filaments

TABLE 2.5.5 CONDUCTOR DESIGN AND ENGINEERING B – SUMMARY

2010 Targets

- < $10 / kA-m
- Throughput processing = 100 m/h
- 0.25 W/ kA-m
- Je > 10^4 A / cm2 at 3T and 65K

Critical Developments

- 2005- Practical joints and field splices
- 2007- Low AC loss
- 2007- Flux Pinning

R&D Activities

- Understand Process/Property/Structure of Jc (B, θ, T)
- Develop a method of making and transposing filaments
- Design and text prototype CC's under device conditions
- Scale-up processing rates and throughput
- Quench- Measure and model stability and thermal protection

Key Messages

- DOE support coordinated activity- CDEI- Conductor Design and Engineering Initiative
- Interface between users and manufacturers
- Broad spectrum of activity
- AC losses and severe transient in devices

3. PRESENTATIONS

3.1 Introduction and Vision

J. Daley
U.S. Department of Energy

Program: Mission and Goals

Mission:

Work in partnership with industry to perform HTS wire and pre-commercial activities required for US companies to commercialize HTS electric power applications

Strategic Goals:

- Achieve HTS wire with 100x current capacity of copper
- Complete prototype demonstrations of HTS electric power equipment such as motors, current controllers, power cables, transformers, and generators

Evolution of the Roadmap

- Research & Development Roadmap – Achieving Advanced Electrical Wires From Superconducting Coatings, November 1997
- Coated Conductor Technology Development Roadmap – Priority R&D Activities Leading to Economical Commercial Manufacturing, August 2001
- Coated Conductor Technology Development Roadmap Workshop II, July 2003

Plenary Session

- Introduction and Vision
- Thought Provoking Perspectives on HTS Coated Conductor Product Needs
- Roadmap Process and Expectations

Breakout Sessions

- Buffers & Substrates
- RE-123 Nucleation, Growth, and Flux Pinning
- Conductor Design & Engineering (A & B)

Plenary Summary Session follows

Vision for the Coated Conductor Development Roadmap

- Low-cost, high-performance HTS coated conductors will be available in 2005 in hundreds of meter lengths.
- For applications in liquid nitrogen, the wire price will be less than $50/kA-m, while for applications requiring cooling to temperatures of 20-60K the price will be less than $30/kA-m.
- By 2010, the price-performance ratio will have improved for kilometer lengths by at least a factor of five.

3.2 Summary MURI Workshop on Fundamental Scientific Issues Underpinning Coated Conductor Development

David Larbalestier
University of Wisconsin-Madison

Summary
MURI Workshop on Fundamental Scientific Issues Underpinning Coated Conductor Development

June 11 and 12, 2003
at the University of Wisconsin-Madison
organized by
David Larbalestier, Malcolm Beasley and Judy Wu
from the
Wisconsin-Stanford-Kansas-Davis MURI
on
"Fundamental Scientific Studies of Coated Conductors"

Workshop Program

Wednesday June 11

Session 1: Review of Key Issues in the 2001 Coated Conductor Roadmap
(Discussion leaders: Mac Beasley, David Larbalestier and Judy Wu)

Session 2: Protection, Stability and Conductor Design
(Organizers: David Larbalestier and Alex Malozemoff)
Key Speakers: Paul Barnes, Robert Duckworth, Alex Malozemoff, and Justin Schwartz

Thursday June 12

Session 3: Growth of the Conductor
(Organizers: Mac Beasley, Bob Hammond and Mas Suenaga)
Key Speakers: Michael Cima, Ron Feenstra, Bob Hammond, and Vlad Matias

Session 4: Vortices in coated conductors
(Organizers: Judy Wu and Dave Christen)
Key Speakers: Dave Christen, Leonardo Civale, Alex Gurevich, and Judy Wu)

Friday June 13

Discussion and report drafting

Discussion participants

Melinda Adams, University of Wisconsin-Madison
Paul Barnes, Air Force Research Laboratory
Malcolm Beasley, Stanford University
Rabi Bhattacharya, UES, Inc.
Ron Bing, Air Force Research Laboratory
James Carr
David Christen, Oak Ridge National Laboratory
Michael Cima, Massachusetts Institute of Technology
Leonardo Civale, Los Alamos National Laborator
Robert Duckworth, Oak Ridge National Laboratory
Ron Feenstra, Oak Ridge National Laboratory
D. (Matt) Feldmann, University of Wisconsin-Madison
Paul Grant, Electric Power Research Institute (EPRI)
Alex Gurevich, University of Wisconsin-Madison
Robert Hammond, Stanford University
Timothy Haugan, Air Force Research Laboratory
Eric Hellstrom, University of Wisconsin-Madison
Sang Il Kim, University of Wisconsin-Madison
Chuhee Kwon, California State University-Long Beach
David Larbalestier, University of Wisconsin-Madison
Yuanyuan Lei, Argonne National Laboratory
Beihai Ma, Argonne National Laboratory
Alexis Malozemoff, American Superconductor Corporation
Kenneth Marken, Oxford Instruments
Vlad Matias, Los Alamos National Laboratory
David Mattox, MicroCoating Technologies
Ruling Meng, University of Houston
Dean Miller, Argonne National Laboratory
Charles Oberly, Air Force Research Laboratory
Anatolii Polyanskii, University of Wisconsin-Madison
Jodi Reeves, SuperPower Inc.
Noel Rutter, University of Cambridge
Kamel Salama, University of Houston
Justin Schwartz, Florida State University
David Shaw, SUNY-Buffalo
Xueyan Song, University of Wisconsin-Madison
Masaki Suenaga, Brookhaven National Laboratory
Mike Sumption, Ohio State University
Susana Trasobares, Argonne National Laboratory
Harold Weinstock, AFOSR/NE
Judy Wu, University of Kansas
Yi-Yuan Xie, SuperPower Inc.

Industry - National Laboratories – Universities - Government

Update for DOE CC Road Map Workshop July 28-29, 2003 MURI CC Workshop Summary: June 11-12, Madison WI

Message and Intended Audiences

Coated conductors with attractive properties are being made by continuous processes now

BUT

only long term work on developing a fundamental understanding of their processing, their properties and the inter-relations between them will ensure that Coated Conductors can enter the commercial market place with the low price/performance properties needed to replace copper and iron in electro-technology.

1. The applications community at DOE-EERE, the DOD and DOE national laboratories, and their industrial user base for high temperature superconducting wires and tapes
   - the July 2003 DOE post-Peer Review road-mapping exercise
   - broader military users including DARPA
2. The basic science community at DOE-BES, NSF, AFOSR and elsewhere
3. The worldwide community of coated conductor developers

Update for DOE CC Road Map Workshop July 28-29, 2003 MURI CC Workshop Summary: June 11-12, Madison WI

The Conductor

- The conductor
  - Vital need for **J_e enhancement (T_c, J_c (T, H, θ), thicker)** for magnets and J_e per unit width for cables*, desirability of AC loss reduction especially for high frequency military use (subdivision, percolation), protection (the big issue), stability (perils of too much), strength (conductor architecture tradeoffs)
- High priorities
  - Develop better understanding of **conductor**/magnet protection** under typical HTS conditions of very slow quench propagation and large stability margins
  - Develop understanding of the **flux flow resistivity of CC** so as to be able to predict current transfer to stabilizer in presence of normal zone
  - Understand **protection issues and relation to "defects"** as well as average performance
  - Understand **AC loss properties in CC** and develop appropriate experimental techniques and model/simulations
  - Approaches to **transposed and/or filamentary geometries** and/or design magnets for tape conductor use, especially under AC operation at frequencies up to 2kHz
  - Usefulness of **targets for the conductor** – e.g. 1000A/cm for enhanced Je performance and narrow conductors, e.g. 1-2 mm wide conductors for tests of transposability and lower loss

*Transmission line and transformer metric is Ic(A/m) factor. Je is applicable for magnets.

** Protection issues are different for magnets versus cables and transformers. Magnet protection is dominated by stored energy but cables by their short-time but very high over-currents and need to avoid cable quench.

YBCO Growth

- YBCO growth
  - The vital **role of liquid** for high growth rates (nucleation and growth), through-thickness microstructure variations, other RE-123 compounds or partial substitutions
  - **Precipitates, interfaces and grain boundaries**
  - **Development of microstructure** and its significance for Ic and mechanical properties
  - **Process control tools**
- High priorities
  - Understand **phase stability** under process conditions relevant both for high vacuum and "chemical, higher-pressure" routes
    - Understand role of liquid in controlling desired properties
    - Understand reactions with seeds and buffers and their consequences
  - **Systematic microstructural studies** by SEM and TEM for relevant length scales and properties
    - Understand microstructure evolution and connect to Jc (distinguish flux pinning and connectivity effects)
  - **Build understanding of GBs and interfaces at atomic level**
    - Connect theory and experiment at needed levels of complexity and use to ameliorate properties by doping or chemical substitution
  - **Explore the higher-Tc 123 systems**, e.g. Nd-123
    - Understand added temperature and field margins
  - **Develop the detailed scientific understanding needed for CC processing**

Jc, flux pinning and thickness effects

- Jc issues
  - Underlying physics of **vortex pinning in the 2D and 3D limits** and the need for good tests of what regime CC are in
  - Great present variety of experimental results on the **thickness-dependence of Jc** and the striking disagreement between thinned samples and those of variable thickness
  - **Angular dependence of Jc** and implications for flux pinning and magnet use
  - **Interface and grain boundary effects**, their lessening effect at higher field and temperature and practical means to mitigate such effects
  - Texture, vicinality, porosity, precipitations and lack of definable connection to Jc properties
- High priorities
  - Complete **understanding of Jc-thickness** affects vital to high J_e conductor development
  - Test what **flux pinning physics** applies and how much the extensive microstructural variability seen in various designs of CC matters
    - In particular is the dominant pinning mechanism random or correlated?
    - Systematic measurements of Jc(H,T,θ) to evaluate flux pinning and for engineering design
    - Establish sources of pinning by detailed microscopy and connection to growth process
  - **Measurements at various length scales to understand connection of global to local measurements**
    - Comparison of MO, LTSLM and Hall probes at scales of 0.1-10 μm, push to higher fields
    - Comparison of differing microstructures and search for quantifiable defects and direct correlations to Jc
  - Understand the **relationships between intra- and inter-grain Jc over wider H and T ranges**
    - Understand the connections to texture and conductor architecture and fabrication method

Important basic issues not discussed in depth

- **Substrates and strength/conductivity tradeoffs**
- **Buffers, especially conductive ones**
  - Broad issues of flexible processing, compatibility with YBCO (or other 123) remain presently the domain of empirical study – more science for this vital area is needed – remember the S story!
- **Improvement of texture remains vital to high Je at minimum 123 thickness**
  - The importance of granularity in the underlying texture and its relevance to the large grain size contrast between IBAD/ISD and RABiTS approaches
  - Better understanding of IBAD and new materials suitable for fast texture and YBCO growth
- **Stabilizers**
  - Influence of conductor architecture and requirements of power cable or magnet performance
- **Characterization needs**
  - In situ diagnostics for science and process control
- **Thermodynamic data needs**
  - Theory and modeling of nucleation, growth and precipitation
- **Processing difficulties**
  - For obvious reasons process failures are not much discussed either by industry or by the labs – yet rapid progress would be much enhanced by greater openness
- **Process schemes with flexibility**
  - Scale-up and capital cost are vital issues even if all other features for a highly competitive CC are developed
- **The need for effective cross-institutional collaborations**
  - Complexity of the CC requires truly interdisciplinary effort and the need for frequent critique by friendly insider/outsiders

Summary Themes

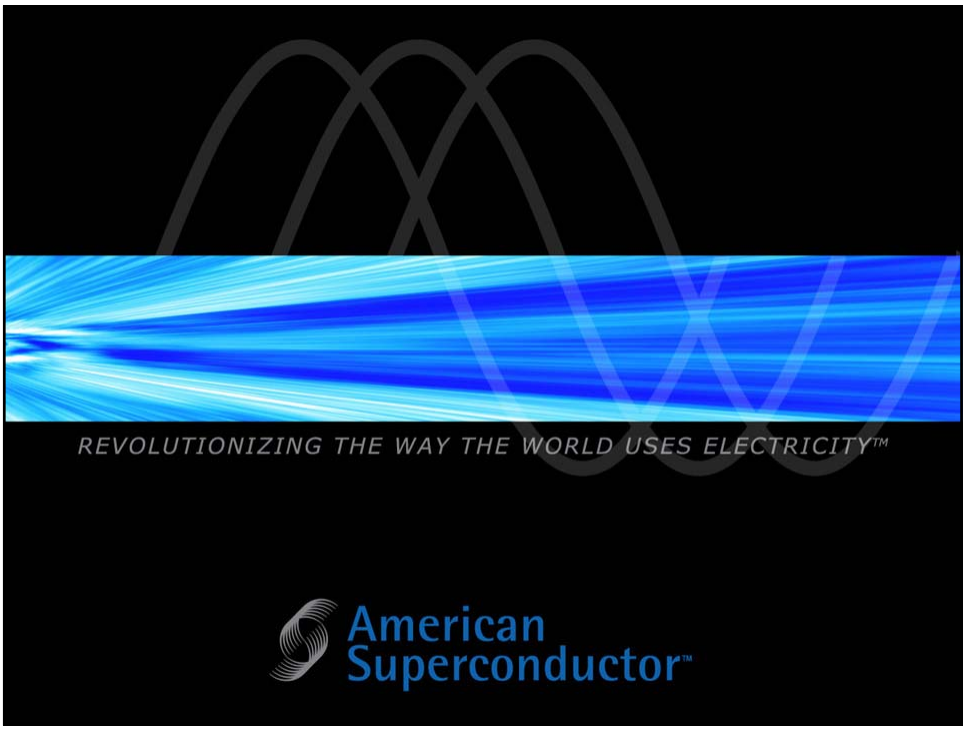
- After about 7 years of R&D, CC are now being successfully scaled-up in industry by continuous processes with properties that can be competitive with Bi-2223
- Widespread acceptance of HTS materials in the utility industry requires a research focus on those developments that will lower cost, enhance performance and match customer needs.
  - The architecture of a CC is complex
  - The superconducting YBCO layer is the penultimate layer and superconductor properties depend on all underlying layers
- Focused discussion of the key problems impeding attractive price/performance targets for widespread acceptance should prioritize R&D
  - The community of researchers has most of the capabilities needed to resolve the open issues that confront this technology
- Military use of CC is essentially different from civilian use, because CC is a technology driver, not a Cu/Fe replacement

Peer Review Update – July 25, 2003

- **Coated conductors are going to happen**
  - AF needs will be met
    - Cost is secondary to performance
  - Will electric utility needs be met?
    - Cost is primary
- **Coated conductors are a series-connected, flaw-dominated technology**
  - Performance
  - Product yield
  - Conductor protection
- **Thorough, fundamental understanding of the whole fabrication-microstructure-property triangle is needed to meet low cost targets**
  - To succeed in replacing Cu and Fe by $YBa_2Cu_3O_{7-x}$ will be an substantial scientific and engineering achievement at the highest level
  - We need connections to our broader communities
  - Need more groups working together

3.3 Revolutionizing the Way the World Uses Electricity

John Scudiere
American Superconductor Corporation



2003 DoE Peer Review

AMSC Commercial Coated Conductor (2G) Wire Program

Coated Conductor Roadmapping Workshop II

July 28, 2003

2

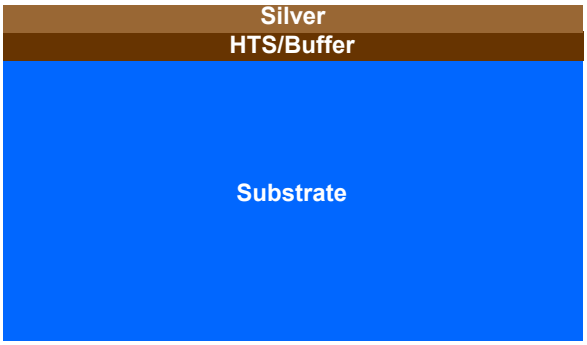
American Superconductor

Outline

- 2G Commercial Wire Geometries
- Proposed Industry Standard Specs
- Next Step for Scale-up
- Key Performance Challenge – community need

American Superconductor

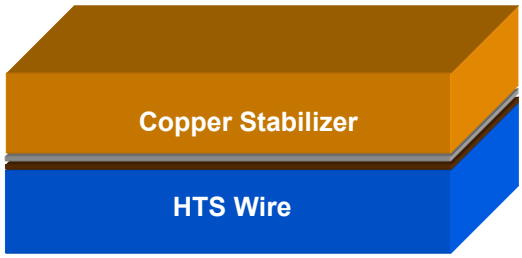
Wire Geometry
Basic RABiTS™ / MOD 2G Wire Architecture



But need to add stabilizer layer to create commercially viable wire!

American Superconductor

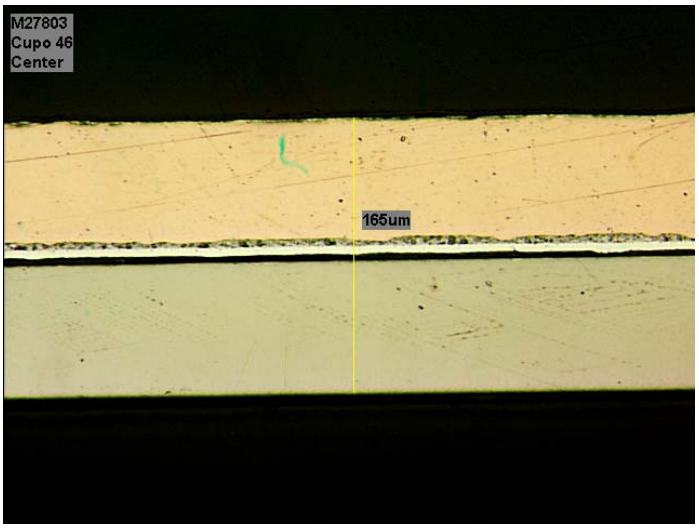
AMSC Neutral Axis 2G Wire Architecture



- Optimum bend properties
- Easy electrical joints and contacts
- High Je

American Superconductor

Neutral Axis Wire Cross-Section



Copper Stabilizer

Solder
Silver Cap
HTS
Buffer Layers

NiW Substrate

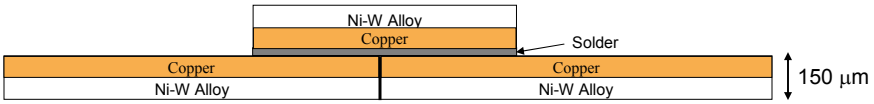
American Superconductor

Neutral Axis Wire Splice – meets 1G specification

A splice can be fabricated by making two lap joints, each a few cm long

- **Typical 1G Lap Joint Specification is 200 nΩ and has 4 cm² overlap**
- **Tested 2G overlap resistance is approximately 100 nΩ for 1 cm² overlap**

Example: A 10 cm long splice will have two 50 nΩ overlap joints (2 cm²) in series totaling 100 nΩ



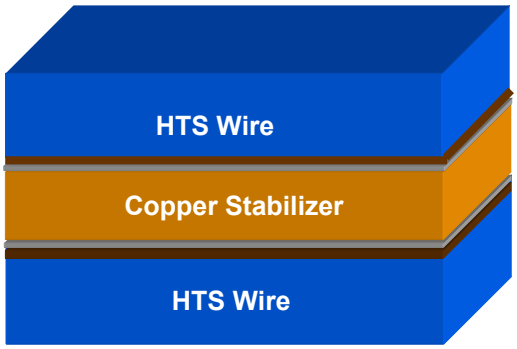
Alternate Neutral Axis Winding (Two-in-Hand)

Neutral Axis 1

Neutral Axis 2

- **Optimum bend properties**
- **Current sharing between HTS layers possible**
- **Easy joints**
- **High Ic and Je**

AMSC Face to Face 2G Wire Architecture



- Current sharing between HTS layers
- High Je
- High Ic

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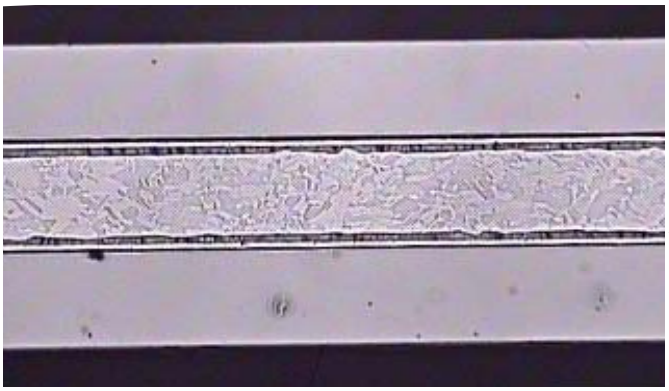
Face to Face (FF) Wire Cross-Section



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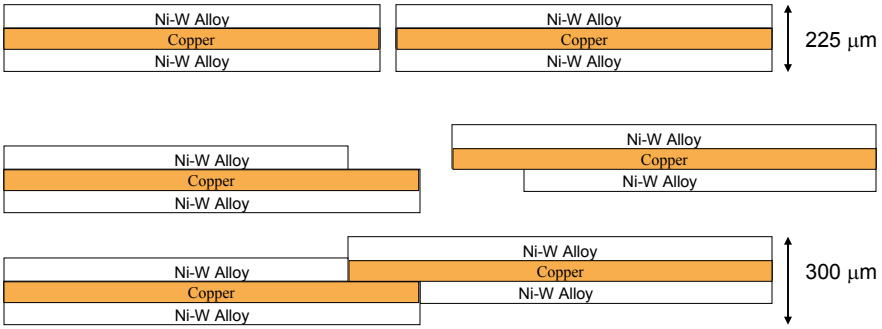
Face - Face Wire Splice

A splice can be fabricated by removing the Ni-W alloy face down to the copper laminate and soldering



Note: Copper stabilizer thickness is easily varied based on application requirements

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Proposed 2G Target Wire Specifications

Geometry:	Face-to-face	Neutral Axis
Ave. width:	4.1mm	4.1mm
Ave thickness:	0.30mm	0.15mm
Min Ic (77K, sf):	240A	120A
Min Je (77K, sf):	20,000 A/cm^2	20,000 A/cm^2
Critical stress long (RT):	150 MPa	150 MPa
Critical stress c-axis (RT):	20 MPa	20 MPa
Critical tensile strain (77K):	0.4% (cyclic 0.3%)	0.4% (cyclic 0.3%)
Critical compressive strain (77K):	0.3% (cyclic 0.2%)	0.3% (cyclic 0.2%)
N-value:	14	14
Min Bend Diameter:	70mm	35mm
Laminate Material:	Copper	Copper
Piece Length:	100 - 1000m	100 - 1000m
Price (large volume):	≤$6/m	≤$3/m

Customers have confirmed targets

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Customer Comments for 2G Specifications

- Eight customers contacted, representing:
  Cables, Motors, Generators, MRI, Specialty Magnets, Coils
- Geometry Preference:
  2 NA, 2FF, 4 Both
- Width Preference:
  3 target 4.1mm ok, 1 target 5mm, 4 want width flexibility
- All customers require Ic vs. B, T data
- 3 customers need insulation and/or splices

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Key Manufacture Scale-up Assumption

10cm wide Process Strip = 20 NA wires = 10 FF wires

Wide processing key to reducing cost

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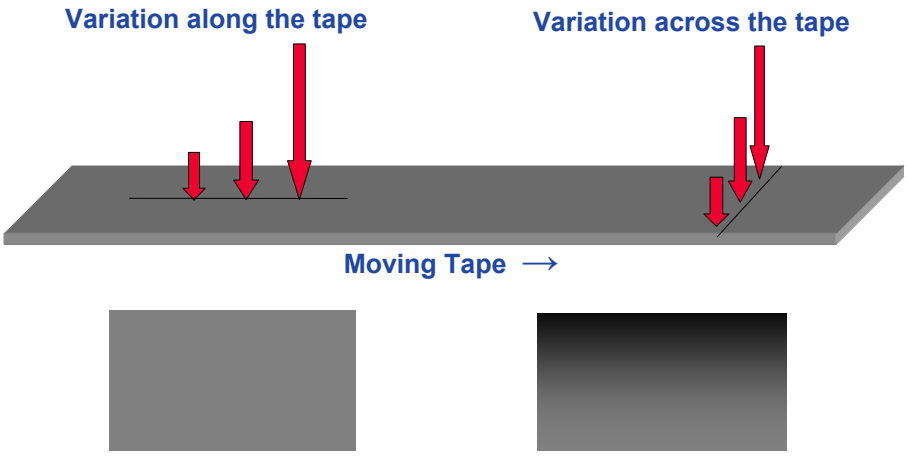
Width Demonstration at interim 4 cm is Next Step for Scale-up



All 2G deposition and reaction processes must demonstrate width uniformity

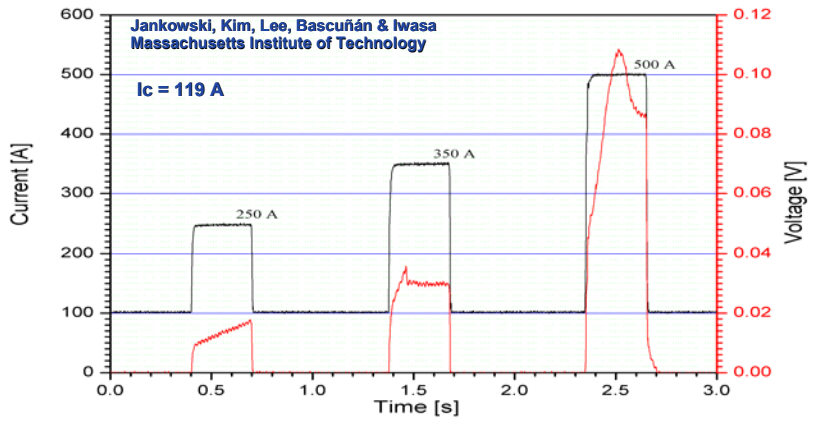
Another Key Step in Preparing for Scale-up

Demonstrate Handling Equipment

- Pay-off
- Take-up
- Camber
- Leveling
- Leader Joints
- Spools
- Transport
- Storage
- Tension Control
- Contamination Control
- Environmental Control

What is easy for a few kg can be difficult at 100s of kg

Issues: How much stabilizer is needed for each application? Alternate coil protection options?



- Recovers from over-currents > 4 x Ic with 300 ms hold-time
- MIT is establishing recovery limits of current & hold-time

MIT

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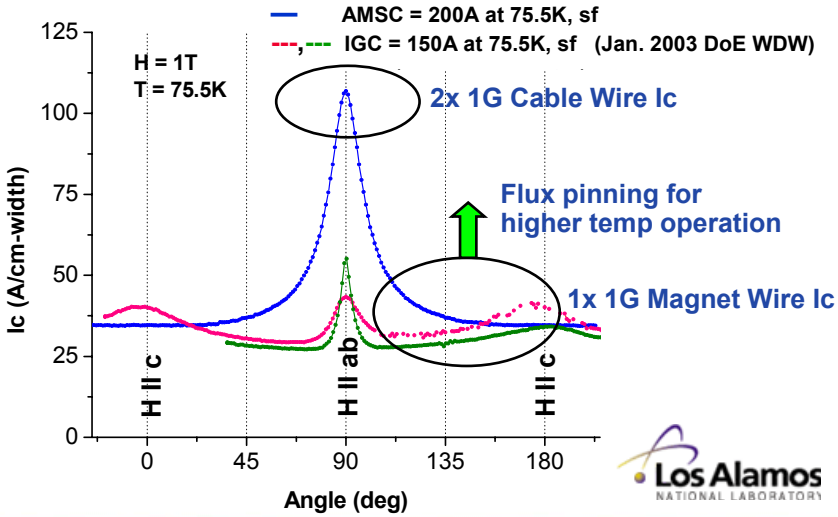
Challenge for the Community – pre-competitive R&D : Flux pinning

Assume 240A min Ic @ 77K, sf



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Electrical Performance Implications

- Commercial Ic (minimum) target: 240A (77K, sf)
  = 2 x 300A/cm-w
  need margin: >2 x 350A/cm-w (average)
- Customer wants 100-200A at operating conditions
- Change focus to Je at 0-1 T and 2-3T, 100-200A

Je 20,000 A/cm2	Cables, FCL (~77K)
Je 10,000 A/cm2	Coils (highest temp)

coils need improved flux pinning for higher temp operation

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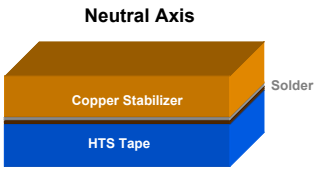
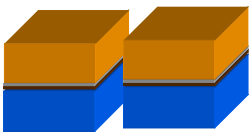
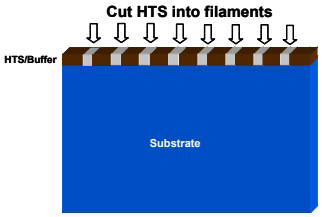
Challenge for community: need to test AC loss reduction solutions

Thin HTS Layer



Narrow Wires





Segmented Filaments
but
Do we need to twist wire?

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Schedule Issues

- R&D equipment is not suited for real SPI demo manufacture (length and quantity output).
- Pilot equipment will require 12-18 months to commission.
- Government support is required to establish rapid Pilot capability.
- Title 3 will potentially start Pilot in July 2004.
- Significant quantities (2-300m to 1000m length) initially available late 2006/beginning 2007.
- Significant 2G SPI application demonstrations in 2008.

Significant SPI demonstrations require Pilot funding start in CY2004

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Summary

- Need to demonstrate commercial wire width (not 1cm).
- Need to adopt standard commercial specification.
- Need to understand wire and coil stability - demos.
- More flux pinning needed for higher temperature coil operation.
- Need to understand ac losses vs. options for improvement.
- Government support required for Pilot capability:

Pilot support CY2004 → Significant SPI wire in CY2006/7
Significant SPI wire in CY2006/7 → SPI demos in CY2008

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End

REVOLUTIONIZING THE WAY THE WORLD USES ELECTRICITY™

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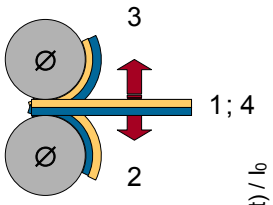
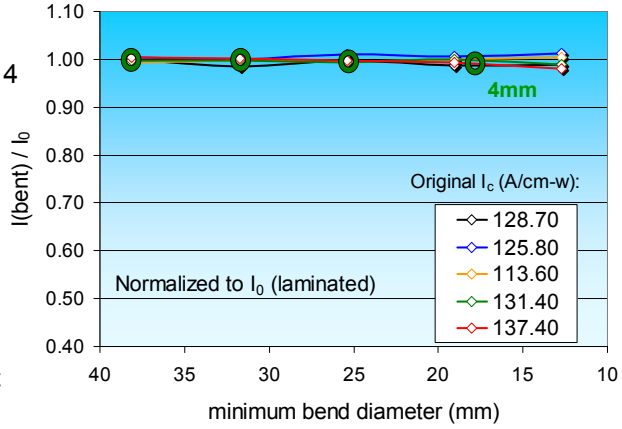
Bend Performance for Neutral Axis Wire



RT bend test

1. Laminate *neutral axis*
2. Bend down
3. Bend up
4. Straighten out

Typical for 10mm and 4mm wide wire



Bend <25 mm with >95% Ic retention

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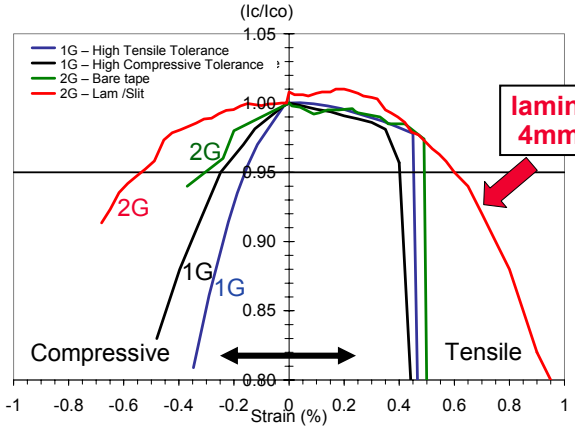
Critical Strain Tolerance of AMSC Wires



Stabilized 2G Critical Strain Tolerance exceeds best 1G performance

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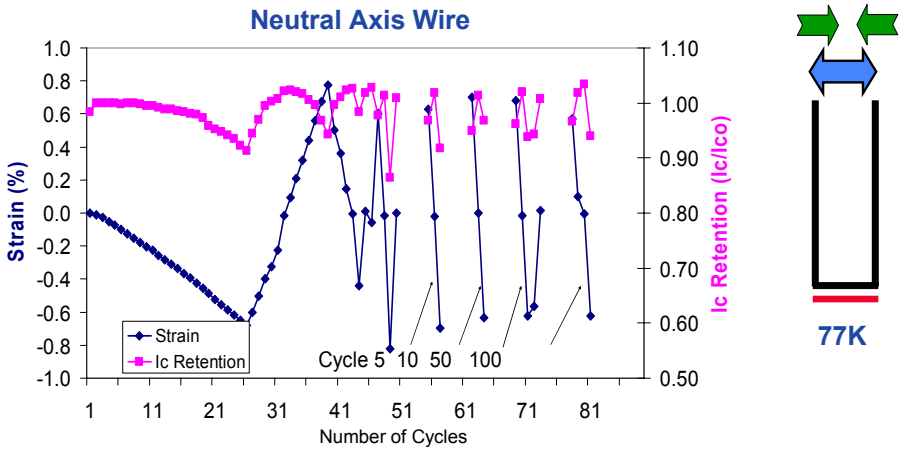
Cyclic Ic/Strain Behavior Laminated and Slit 4mm Wire



Stabilized 2G Critical Strain Tolerance exceeds best 1G performance

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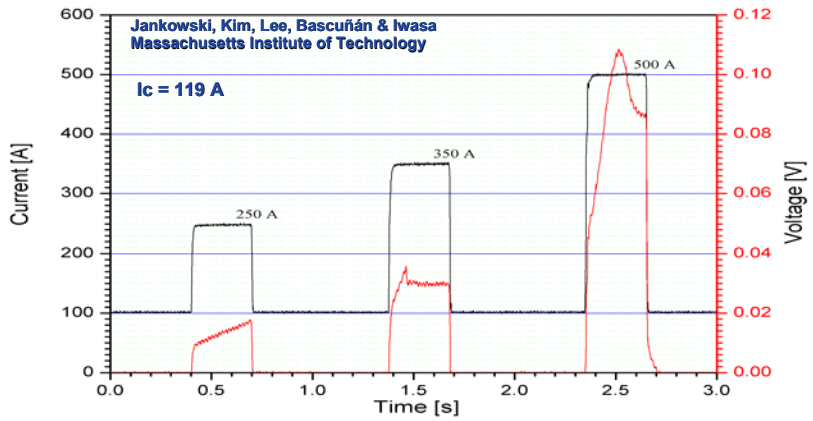
Over-Current Tests of Neutral Axis Wire



- Recovers from over-currents > 4 x Ic with 300 ms hold-time
- MIT is establishing recovery limits of current & hold-time

MIT

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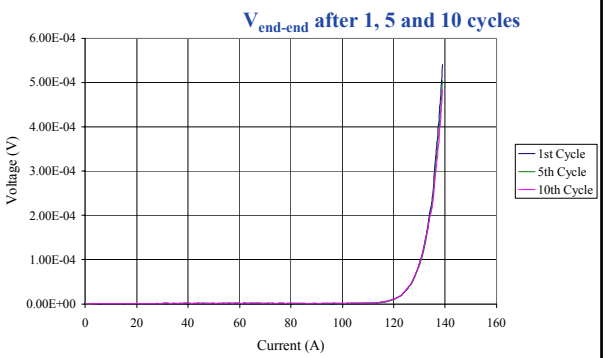
Coils with 1m long Neutral Axis Wire are made using AMSC coil fabrication techniques

- With 142A wire, a coil was fabricated, achieving 50 mT at a coil I_c of 129 A
- Repeated RT-77K cycling shows no change in I_c



Work supported by AFRL

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Significant Findings from FY03 Process Development Work

- **The characteristic length to achieve steady state for all RABiTS/MOD reel-to-reel processes (including PVD buffers) is less than 10 meters.**
- **RABiTS/MOD process shows uniform Ic in 1cm – 1m – 10m lengths (no significant drop observed with increasing length).**
- **Jc in MOD process remains high for increased HTS layer thickness (no precipitous Ic drop observed): Excellent total Ic performance demonstrated.**
- **No fundamental process issues encountered: a very stable process!**
- **Laminated copper significantly increases mechanical properties.**

RABiTS / MOD process is stable, attractive for scale-up

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3.4 Critical Issues to Be Addressed in Coated Conductor Technology

Venkat Selvamanickman
SuperPower, Incorproated

SuperPower Inc.
A Subsidiary of Intermagnetics General Corporation

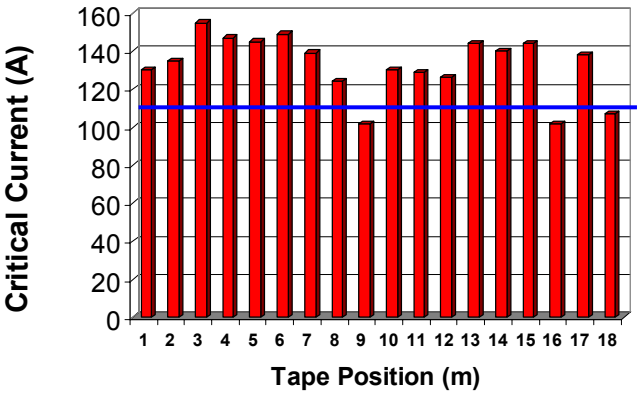
Critical issues to be addressed in coated conductor technology

- Venkat Selvamanickam

HTS Solutions for a New Dimension in Power

DOE wire roadmapping workshop, July 28 - 29, 2003

Rapid Progress in Coated Conductor scale up



111 A over 18 m MOCVD tape ~ 2000 A-m

Timely to evaluate issues with high volume manufacturing

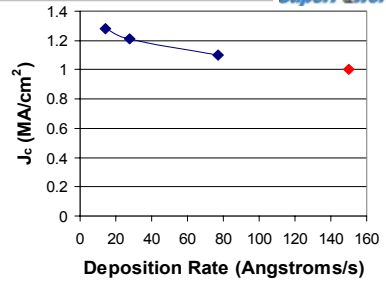
2003 DOE Peer Review –1–

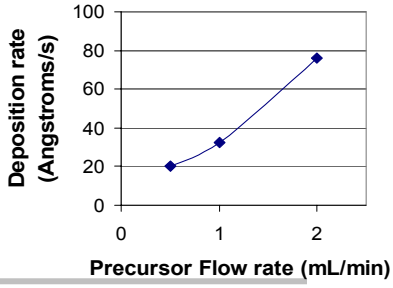
Deposition rates have to be high to produce low-cost conductor

- AMSC stated in the Peer Review that a production of 10,000 km/year of 4 mm wide conductor is needed to reach $ 25/kA-m.
- To reach less than $ 10/kA-m with the same capital base, one way is to increase Ic to 300 A in 4 mm widths.
- Starting with a 10 cm wide tape, need 400 km/year of tape with 8 micron thick YBCO & Jc of 1 MA/cm^2
- Using a 10 m long deposition zone, need a linear tape speed of 65 m/h
- For a 8 micron film, a deposition rate of 150 Angstroms/second would be needed.
- ***150 Angstroms/s has been achieved with MOCVD. 10 m deposition zone is possible with MOCVD. A single MOCVD system can meet the entire Production demand.***
- ***With 10 Angstroms/s rates with ex situ processes, at least 15 systems of capital equipment each with 10 m deposition zone would be needed ($$$$$). Would $ 10/kA-m be possible with such an expensive capital base ???***
- Challenge to the ex situ process developers is to increase the deposition rate further beyond 10 Angstroms/second.
- ***Vacuum levels less than MOCVD (10 Torr) may be needed to achieve higher deposition rates with ex situ processes.***

Even higher deposition rates with MOCVD can shrink the size of capital equipment further

- 150 Angstroms/s has been achieved with MOCVD. 10 m deposition zone is possible with MOCVD. A single MOCVD system can meet the entire Production demand.
- High quality YBCO has been shown with in situ deposition processes (PLD) even at a rate of 650 Angstroms/s
- Potential to improve deposition rate with MOCVD at least up to 650 Angstroms/s. ***At this rate, a single MOCVD system with a 2.5 m deposition zone would be needed to meet the production demand.***
- Rate of 650 Angstroms/s in PLD was limited only by laser power.
- ***No limit for precursor supply in a MOCVD process. Would rates even higher than 650 Angstroms/s possible ?***





In situ processes enable multiple passes to reduce process cycle times

SuperPower

Short process cycle times not only desired to produce longer lengths & low-cost conductor, but also to increase the process reliability

Multiple Pass Process by MOCVD

First Pass: Deposit first *half* thickness of HTS layer

↓

Second Pass: Deposit second *half* thickness of HTS layer

↓

120A over 1 meter

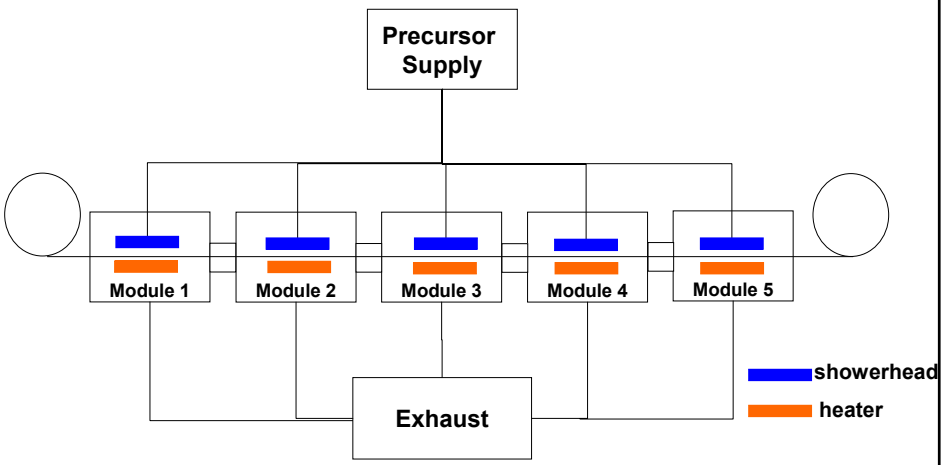
No Ic degradation even when process cycle time is reduced to 1/2

Multiple passes enabled by In-situ processes allows a modular design

SuperPower

Any module can be taken out of service without interrupting run !

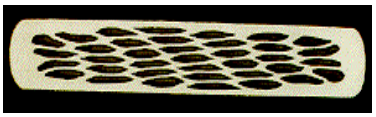
Modules can be added "just in time" to address market demand !



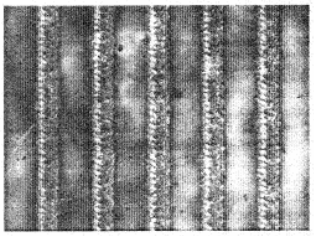
A.C. losses : Substrate influence

SuperPower

Filamentary structure is desired to reduce a.c. losses in superconductors

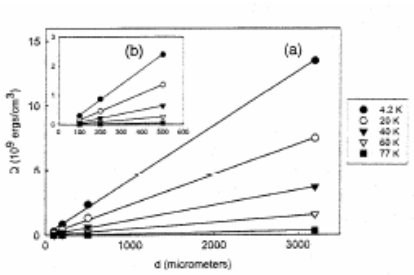


1st gen structure is multifilamentary



Patterning of coated conductors to produce a multifilamentary structure is the only technique proven to reduce a.c. losses

Cobb et al. Physica C. 582, 52 (2002)

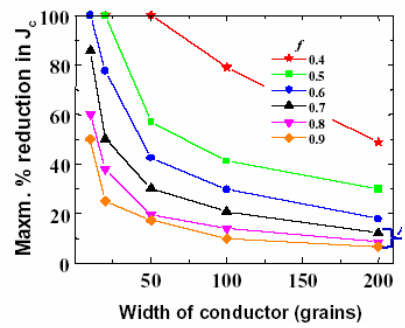


Filamentary conductors may not be possible with substrates with large grains

SuperPower

Assume, # filaments in a 4 mm wide conductor = 30

Width of each filament = 100 microns



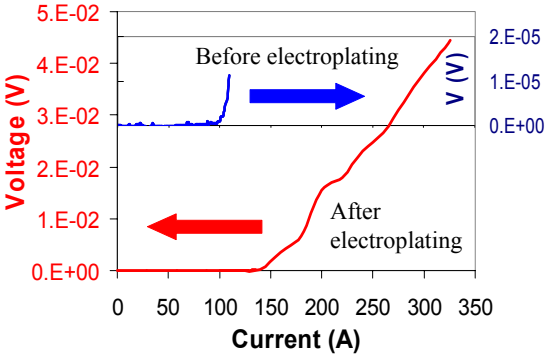
Specht et al. Supercond. Sci. & Technol. 13, 592 (2000)

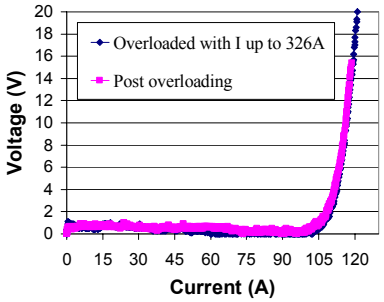
For a 100 micron wide filament,

Grain size (microns)	40	1
# grains/filament	2.5	100

- **Extensive pinch-off could occur in coated conductors with large grains**
- **Alternate techniques may have to be developed for reducing a.c. losses in conductors with large grains.**

Electroplating demonstrated as a viable technique for copper stabilizer application



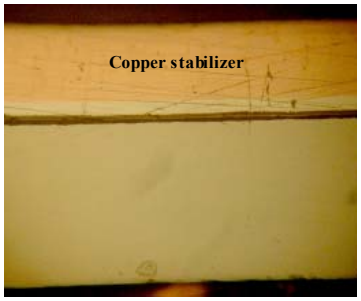


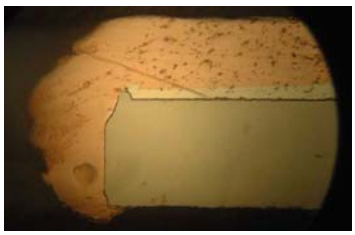
No loss in critical current after electroplating copper stabilizer.

Electroplated tape overloaded to three times Ic (326 A) & 1000 times higher voltage

No change in critical current when retested after overloading to 326 A

Conductor has to be designed for the high voltage applications (138 kV+)





Conductors with sharp corners may not be desirable for high voltage applications

First-generation HTS conductor has rounded edges !

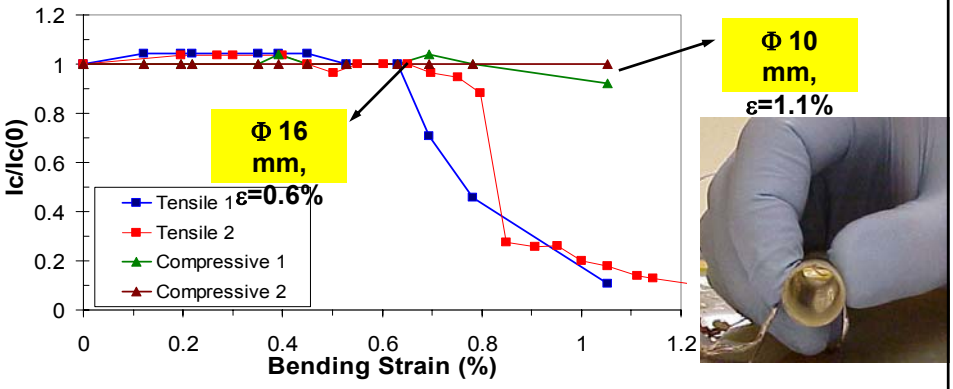
- Electroplating rounds off sharp edges
- Double sided coatings and complete side wall coverage in a single pass

Bend strain effect on Ic is critical for cable applications

SuperPower

HTS cable produced by Sumitomo Electric Industries has a 16 mm core.

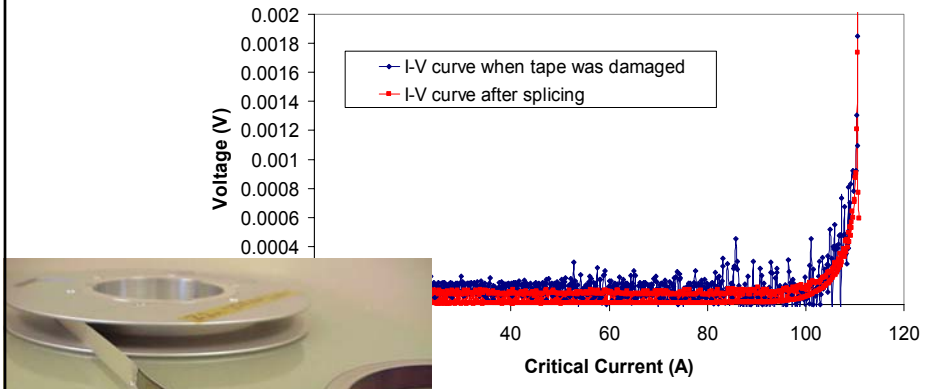
Second-gen tape should be able to bent around 16 mm diameter without Jc degradation.



Need further work on bend strain effect on Jc, especially with thicker HTS films

Damaged sections can be repaired by splicing

SuperPower



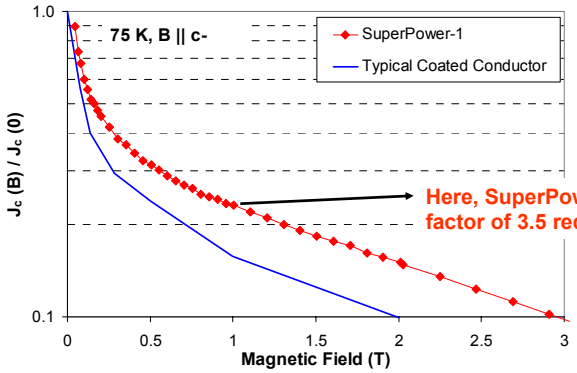
Ic across splice same as virgin conductor

I-V curve is less noisy after splicing !

To Achieve 100 A @ 1 T : Development of a Coated Conductor with Better Magnetic Field Performance

Jc of typical coated conductor with Jc ~ 1 MA/cm^2 at zero field, reduces by a factor of 7 to 10 at 1 T.

Starting with a 100 A conductor, the Ic at 1 T would then be only 10 - 15 A



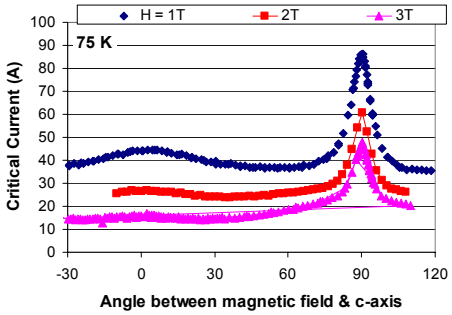
Measurements by Leonardo Civale

Los Alamos NATIONAL LABORATORY 1943-2003

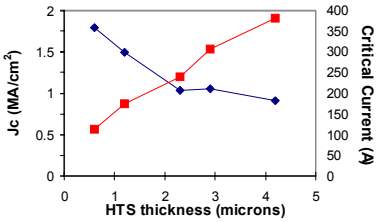
Here, SuperPower tape shows only a factor of 3.5 reduction in Jc at 1 T.

All SuperPower tapes have shown reduction of less than a factor of 4 at 1 T
This is 2 times better performance in field than a typical coated conductor

Jc at B || a-b is proportional to zero field Jc ; Jc at B || c is not !



Starting with a 1.7 micron thick, 167 A tape at 77 K, zero field,
Ic at 1 T, B || a-b = 87 A (1.9 reduction)
Ic (1 T, B || c) = 45 A (3.7 reduction)
Ic (0.1 T) ~ 150 A (for cable applications)



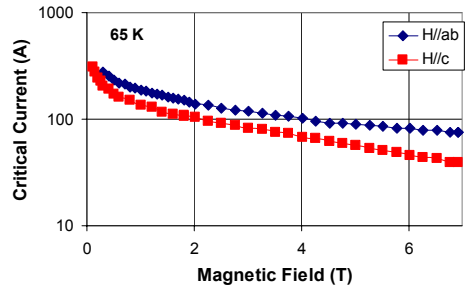
Jc (B || a-b) is determined by intrinsic pinning from the Cu-O planes.
Ic (B || a-b) depends on zero field Ic

Ic = 380 A, Jc = 0.91 MA/cm^2 at 4.2 μm

For most applications, Jc (B || c) is the limiting factor. Jc (B || c) can be improved by extrinsic means

For a Ic (0) = 380 A,
Ic (1 T, B || a-b) = 200 A ;
Ic (0.1 T) ~ 350 A (for cable applications)

100 A at 2 T (B || c) has been achieved at liquid nitrogen temperature with a nominal zero field Ic !



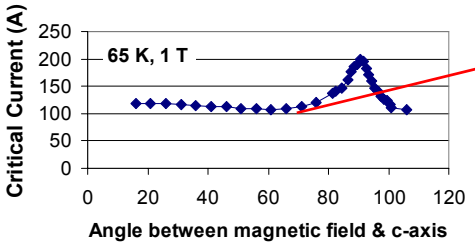
Starting with a 1.7 micron thick, 167 A tape at 77 K, zero field, we have at 65 K :

103 A at 2 T, B || c

135 A at 1 T, B || c

Measurements by Leonardo Civale

Los Alamos NATIONAL LABORATORY 1943-2003



107 A at 1 T, any field orientation

Through extrinsic means, it is possible to achieve high Ic at B || c & intermediate field orientations starting with nominal Ic at zero field!

2003 DOE Peer Review – 14 –

Important to further explore in-field performance of coated conductors

- **HTS conductors produced by *in-situ* processes could be favorably affected by possible flux pinning created by energetic species in the vapor phase.**
- ***Are HTS conductors produced by vapor phase techniques (in-situ process) perform differently in field than non-vapor phase (ex-situ process) produced HTS conductors ?***
- **All 100 A (zero field) coated conductors may not be created equal !**
- **Zero field performance may not present true capability of wire for applications where field is close to c-axis.**
- **Wire customer needs to compare in-field performance of coated conductors produced by different processes**

2003 DOE Peer Review – 15 –

Critical issues with Coated Conductor technology that need discussion

SuperPower

- **How to achieve high deposition rates to reduce capital cost (especially with ex situ processes)**
  - If a low pressure has to be used to achieve high deposition rates in ex situ processes, how does it affect capital cost ?
- **Modular process system design**
- **Are there alternatives to filamentary conductors to reduce a.c. losses using substrates with large grain size**
- **Modifications to present conductor geometry for high voltage applications ?**
- **Retain 100% of Jc when conductor is bend to 16 mm diameter**
- **Splicing to repair damaged conductors**
- **High Ic at 1 T, with field perpendicular to tape surface for a nominal zero field performance.**
  - State not only zero field Ic, but Ic at 1 T, with field perpendicular to tape surface & minimum Ic with field in any orientation.

3.5 Coated Conductors: A Magnet Perspective

Ken Marken
Oxford Instruments Superconducting Technology

Coated Conductors: A Magnet Perspective

Ken Marken and Chris Friend

Oxford Superconducting Technology
Carteret, New Jersey
Oxford Instruments Superconductivity
Eynsham, England

General Comments

- Conductor geometry and specs will depend on particular applications.
- Form-fit-function replacements for 1G HTS may be a good starting point, but we need to think more broadly than this.
- In terms of commercial successes, there are lessons to be learned from LTS.
- Successful applications require conductor manufacturers to work closely with system and product developers.
- Modeling along with component and prototype testing can enable refinement of conductor specifications. These exercises require assessment of economics as well as technical performance.

Superconducting Technology

Magnet Requirements

- Transport Performance: High J_E and I_c are more important than just high J_c.
- Geometry:
  - Wide tapes are not ideal for magnet applications.
  - If tape is necessary, < 4mm wide is preferred.
  - Maximum thickness is dictated by bend requirements, for magnets the range required is ≥ 40 mm diameter.
- Length: > 1 km needed for layer wound coils, for pancake coils shorter piecelengths may be acceptable.
- In present high field magnets the conductor is graded (in type and size) by field region in order to minimize conductor costs.
- Ferromagnetic substrates are undesirable for magnet applications.

OXFORD INSTRUMENTS
Superconducting Technology

Magnet Requirements

- Anisotropy:
  - Anisotropy with respect to field in coated conductors is high and appears more complicated than that in BSCCO.
  - Minimum I_c orientation (between 45° and 90°) will be a limiting factor for high field magnets, a design challenge.
  - Are there alternate conductor configurations that minimize this problem, such as square wires?
  - Low field magnets can use flux diverters.

OXFORD INSTRUMENTS
Superconducting Technology

Magnet Requirements

- Conductor Uniformity:
  - This needs to be very good.
  - Poor tape sections 1 mm long in a km length could cause local stability problems, and possibly field uniformity problems.
  - Current distribution across the tape width is equally important and not well understood.
  - Do we have adequate methods of quantifying and controlling uniformity, both along length and width?

OXFORD INSTRUMENTS
Superconducting Technology

Magnet Requirements

- Thermal Stability:
  - Conductor stability is crucial for successful magnets, as well as many other applications.
  - Thermal stability depends on conductor architecture, an area still in early stages of development.
  - There remains much to learn about thermal behavior in coated conductors.
  - What volume and type of stabilizer do we need?
  - Are there economical fabrication methods that allow a range of stabilizer:superconductor ratios? (Present LTS magnets have ratios varying from 1:1 to 10:1, depending on intended use.)

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Superconducting Technology

Magnet Requirements

- Mechanical Properties:
  - Present LTS magnets operate in the range up to 0.4% strain and 300 – 400 MPa stress, and HTS magnet conductors need to address this range.
  - Required bend diameter range is down to 40 mm, and even lower would be useful for feedthroughs and terminations.
  - It is difficult to engineer magnet systems without the ability to twist tapes to change direction easily (without damage).

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Superconducting Technology

Magnet Requirements

- Joints:
  - Joints are required for all applications.
  - Many LTS magnet applications today require persistent current joints.
  - As the design of a conductor is changed, the ability to make excellent joints should always be a factor.

OXFORD INSTRUMENTS
Superconducting Technology

A High Field Magnet Designers Wish List

Conductor needed for a 25 T mixed conductor magnet ($NbTi+Nb_3Sn$+HTS) operating at 2K:

- Coated YBCO conductor
- 2 mm wide X 200 μm thick
- 1 km length
- > 300 MPa critical stress
- > 0.4% MPa critical strain
- Copper stabilizer and demonstrated conductor stability
- Anisotropy: Ic > 400 A at 3 T applied in minimum Ic orientation. (Roughly equivalent to 150 A at 77K, 675 A at 25 T parallel, 2K.)

OXFORD INSTRUMENTS
Superconducting Technology

3.6 Coated Conductor Product Needs Cable Applications

David Lindsay
Ultera

Coated Conductor Product Needs Cable Applications

U.S. Department of Energy
July 2003 Wire Workshop

28-July 2003

David Lindsay
Director, Ultera

Ultera™ A Southwire / nkt cables Joint Venture Southwire WE DELIVER POWER nkt cables ornl

What do we Want?

"Drop-In" replacement for BSCCO

Physical Properties

- Width = ~4.2 – 4.5 mm
- Min Stress Tolerance = ~80 – 100 MPa (95% Ic Ret)
- Min Strain Tolerance = ~0.3% (95% Ic Ret)

Connectivity

- Easy solder joints
  - Tape-to-tape
  - Tape-to-Copper

Ultera™ A Southwire / nkt cables Joint Venture

Connectivity

- How do we get current into and out of these tapes?

- If substrate/buffer layer is non-conductive or highly resistive, there is only one side usable for soldering and passing current to/from YBCO. **Not Desirable**

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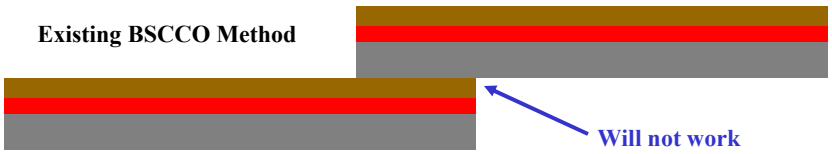
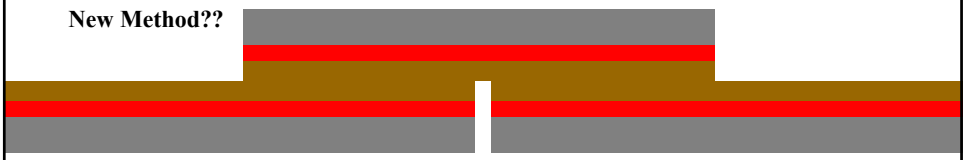
Connectivity – Tape Splices / Repair Joints

Existing BSCCO Method



New Method??



More Complicated.
Longer time to assemble.
2 joints vs. 1 joint.

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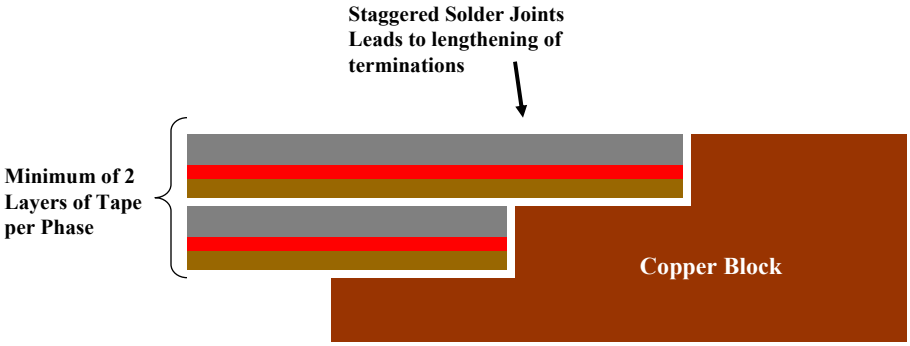
Connectivity - Terminations



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Delivery Schedule

- **5-m Cable – Spring/Summer 2004**
  - Coax = ~750m tape (25-30m piece lengths)
  - Triax = ~1.4 km tape (45-50m piece lengths)
  - Cost = 2x BSCCO price
- **30-m Cable – Fall/Winter 2005**
  - Coax = ~4.1 km tape (~140m piece length)
  - Traix = ~6.2 km tape (~210m piece length)
  - Cost = 1x BSCCO price

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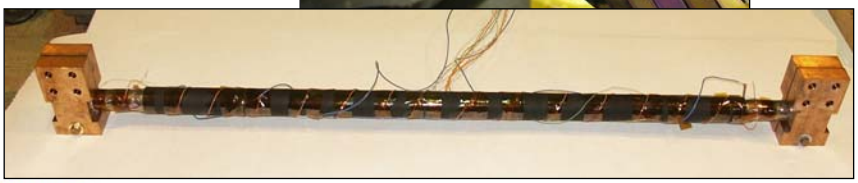
2nd Generation, YBCO - Cable

- 30x 1.5-m lengths of YBCO delivered to Southwire
- Conductor stranded at Southwire and tested at ORNL

dc-Ic = ~4200A
AC Loss = ~2 W/m @ 2 kA



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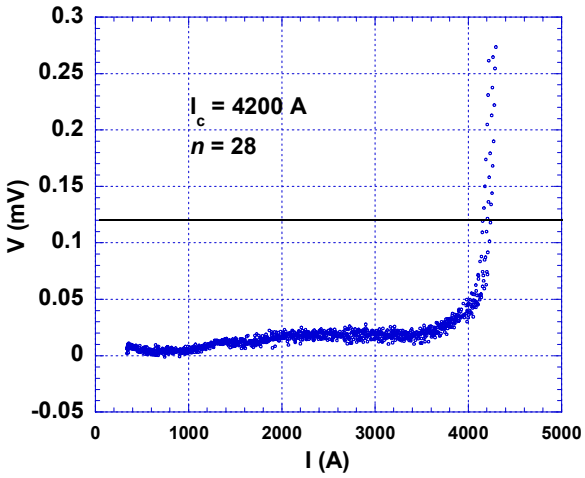
V-I Curve & Over-Current Response



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3.7 Facilitated Gameplan Coated Conductor Technology Development Roadmap

Joseph Badin
Energetics, Incorporated

Coated Conductor Technology Development Roadmap II

Facilitation "Game Plan"

and Meeting Logistics

Joseph Badin
Energetics, Inc.
July 28-29, 2003

Why We're Here

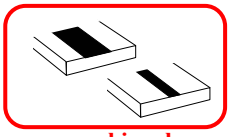
- Purposes
  - Discuss the characteristics and performance targets of the 2010 envisioned engineered HTS coated conductor product
  - Discuss critical technical breakthroughs and key scale-up opportunities to achieve the envisioned product
  - Identify priority R&D activities
  - Identify significant milestones (2005-2010) that need to be achieved for the vision to be realized
- Non-purposes
  - Not to re-create past discussions

Conductor Design & Engineering Initiative:

Bridging the gap between tape fabrication and cable manufacturing

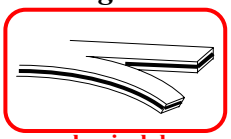
From tape

Percolation…



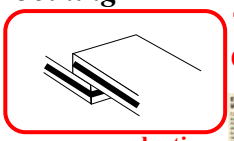
…masking, laser scribing

Slitting…



…mechanical, laser, jet

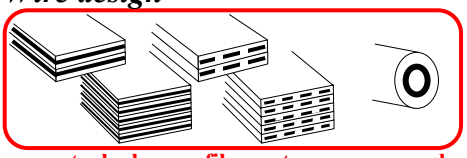
Joining



…superconducting, metallic

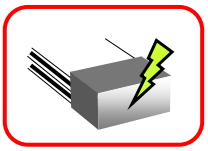
… to cable

Wire design



…stacked, filaments, round

Termination



ETC…

What We'll Do

Day 1

- Plenary session
- Four breakout group sessions
- Luncheon
- Continue breakout group sessions

Day 2

- Reconvene in breakout groups
- Plenary session: group"report-outs" and Q&A
- Discussion of crosscutting themes and final thoughts

Workshop Roles and Responsibilities

- ***Facilitators*** – Leads breakout session, responsible for process, not content. Afterwards, assists with writing and editing the workshop proceedings
- ***Participants*** – Provides ideas in response to focus questions posed by facilitator, can volunteer to be a scribe or spokesperson in the breakout sessions, may have volunteered to be a speaker
- ***Listeners*** – Listens to discussions, can contributes ideas in writing after the meeting

Storyboarding Process - Visionary –

- *Problems become Challenges*
- *Barriers become Opportunities*
- *Delays become Decision making points and*
- *Hard work becomes Fun*

Ground Rules

- Think of the future… ***be visionary***
- Offer "leap frog" ideas… ***be creative***
- Refrain from speech making… ***be concise***
- No attribution of people to ideas… ***be candid***
- Think nationally, not parochially… ***be patriotic***
- Turn off cell phones and beepers… ***be polite***
- No "gunny sacking"… ***be collegial***
- ***Have fun!***

4. PARTICIPANTS

Joseph Badin
Assistant Vice President
Energetics, Incorporated
7164 Gateway Drive
Columbia, MD 21046
Phone: 410-290-0370
Fax: 410-290-0377
Email: jbadin@energetics.com

Paul Barnes
Superconductivity Team Leader
Air Force Research Laboratory
AFRL/PRPG, Building 450
2645 Fifth Street
Suite 13
Wright-Patterson AFB, OH 45433-7919
Phone: 937-255-4410
Fax: 937-656-4095
Email: paul.barnes@wpafb.af.mil

Malcolm Beasley
Professor
Stanford University
Laboratory for Advanced Materials
McCullough 362
Stanford, CA 94305-4045
Phone: 650-723-1196
Fax: 650-725-2189
Email: beasley@stanford.edu

Paul Berdahl
Physicist
Lawrence Berkeley National Laboratory
1 Cyclotron Road, MS 70-108B
Building 70, Room 108B
Berkeley, CA 94720
Phone: 510-486-5278
Fax: 510-486-7303
Email: phberdahl@lbl.gov

Raghu Bhattacharya
Team Leader and Senior Scientist
Basic Science
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401
Phone: 303-384-6477
Fax: 303-384-6432
Email: raghu_bhattacharya@nrel.gov

Dan Brewer
Energy Analyst
Energetics, Incorporated
7164 Gateway Drive
Columbia, MD 21046
Phone: 410-290-0370
Fax: 410-290-0377
Email: dbrewer@energetics.com

Ross Brindle
Energetics, Incorporated
7164 Gateway Drive
Columbia, MD 21046
Phone: 410-953-6239
Fax: 410-290-0377
Email: rbrindle@energetics.com

Claudia Cantoni
Staff Researcher
Oak Ridge National Laboratory
1 Bethel Valley Road
MS-6061
Knoxville, TN 37831
Phone: 865-574-6264
Fax: 865-574-6263
Email: cantonic@ornl.gov

Louis Castellani
President
Metal Oxide Technologies, Incorporated
8807 Emmot Road
Suite 100
Houston, TX 77040
Phone: 832-243-0917, Ext. 10
Fax: 832-243-9536
Email: louis.castellani@metox.biz

Harbans Chhabra
Superconductivity Program
U.S. Department of Energy
1000 Independence Avenuenue, S.W.
Washington, DC 20585
Phone: 202-586-7471
Fax: 202-586-5860
Email: harbans.chhabra@hq.doe.gov

Najib Cheggour
Physicist
Magnetic Technology Division
National Institute of Standards and Technology - Boulder
325 Broadway
Mail Stop 816.02
Boulder, CO 80305
Phone: 303-497-3815
Fax: 303-497-5316
Email: cheggour@boulder.nist.gov

David Christen
Group Leader
Condensed Matter Sciences Division
Oak Ridge National Laboratory
1 Bethel Valley Road
MS 6061
Oak Ridge, TN 37831
Phone: 865-574-6269
Fax: 865-574-6263
Email: christendk@ornl.gov

Paul Chu
Professor of Physics
Texas Center for Superconductivity
University of Houston
202 Houston Science Center
Houston, TX 77204-5002
Phone: 713-743-8222
Fax: 713-743-8201
Email: cwchu@uh.edu

Lawrence Cook
Research Chemist
Ceramics Division
National Institute of Standards and Technology
MATLS B346
Gaithersburg, MD 20899
Phone: 301-975-6114
Fax: 301-975-5334
Email: lawrence.cook@nist.gov

James Daley
Superconductivity Program
Office of Electric Transmission and Distribution
U.S. Department of Energy
1000 Independence Avenue, S.W.
Washington, DC 20585
Phone: 202-586-1165
Fax: 202-586-5860
Email: james.daley@ee.doe.gov

Stephen Dorris
Engineer
Argonne National Laboratory
9700 South Cass Avenue
Argonne, IL 60439
Phone: 630-252-5084
Fax: 630-252-3604
Email: dorris@anl.gov

Kathleen Dunn
Assistant Professor
Albany NanoTech
State University of New York
251 Fuller Road, CESTM
Albany, NY 12203
Phone: 518-437-8686
Fax: 518-437-8687
Email: kdunn1@uamail.albany.edu

Melissa Eichner
Senior Program Manager
Energetics, Incorporated
7164 Gateway Drive
Columbia, MD 21046
Phone: 410-953-6234
Fax: 410-290-0377
Email: meichner@energetics.com

Jack Ekin
Physicist
Magnetic Technology Division
National Institute of Standards and Technology - Boulder
325 Broadway
Mail Stop 816.02
Boulder, CO 80305
Phone: 303-497-5448
Fax: 303-497-5316
Email: ekin@boulder.nist.gov

Ron Feenstra
Senior Research Staff
Solid State Division
Oak Ridge National Laboratory
Building 3137, Mailstop 6057
P.O. Box 2008
Oak Ridge, TN 37831
Phone: 865-574-4341
Fax: 865-576-8135
Email: feenstrar@ornl.gov

Les Fritzemeier
Metal Oxide Technologies, Incorporated
8807 Emmott Road
Suite 100
Houston, TX 77040
Phone: 832-243-0917, Ext. 10
Fax: 832-243-9536
Email: lfritzemeier@earthlink.net

Roland George
Superconductivity Program
U.S. Department of Energy
1000 Independence Avenuenue, S.W.
Washington, DC 20585
Phone: 202-586-9398
Fax: 202-586-5860
Email: roland.george@hq.doe.gov

Brady Gibbons
Technical Staff Member
Los Alamos National Laboratory
P.O. Box 1663
MS T004
Los Alamos, NM 87545
Phone: 505-663-5563
Fax: 505-663-5550
Email: gibbons@lanl.gov

Donald Glenn
Senior Associate
Bob Lawrence and Associates, Incorporated
345 South Patrick Street
Alexandria, VA 22314
Phone: 703-836-3654
Fax: 703-836-6086
Email: dglenn10@erols.com

Robert Hawsey
Manager, Superconductivity Program
Oak Ridge National Laboratory
P. O. Box 2008
MS-6195
Oak Ridge, TN 37831-6195
Phone: 865-574-8057
Fax: 865-574-6073
Email: hawseyra@ornl.gov

Eric Hellstrom
Ceramics Group Leader
Applied Superconductivity Center
University of Wisconsin
1500 Engineering Drive
911 Engineering Research Building
Madison, WI 53706
Phone: 608-263-9462
Fax: 608-263-1087
Email: hellstrom@engr.wisc.edu

Terry Holesinger
Staff Scientist
Materials Science and Technology
Los Alamos National Laboratory
MS G755
Los Alamos, NM 87545
Phone: 505-667-2911
Fax: 505-667-5268
Email: holesinger@lanl.gov

Alex Ignatiev
Director
TcSAM
University of Houston
202 UH Science Center
Houston, TX 77204-5002
Phone: 713-743-8215
Fax: 713-743-8201
Email: ignatiev@uh.edu

Dirk Isfort
Nexans SuperConductors
Chemiepark Knapsack
Hueith, Germany 50351
Phone: 49-223348632
Fax: 49-223348685
Email: dirk.isfort@nexans.com

Vladimir Kogan
Strategic Technology Consultant
American Electric Power
1 Riverside Plaza
Columbus, OH 43215
Phone: 614-223-1231
Fax: 614-223-1292
Email: vikogan@aep.com

Donald Kroeger
Group Leader
Oak Ridge National Laboratory
P.O. Box 2008
Oak Ridge, TN 37831
Phone: 865-574-5155
Fax: 865-574-7659
Email: kroegerdm@ornl.gov

David Larbalestier
Director
Applied Superconductivity Center
University of Wisconsin
1500 Engineering Drive
915 Engineering Research Building
Madison, WI 53706
Phone: 608-263-2194
Fax: 608-263-1087
Email: larbales@engr.wisc.edu

Lloyd Lawrence, Jr.
President
Bob Lawrence & Associates, Incorporated
345 South Patrick Street
Alexandria, VA 22314
Phone: 703-836-3654
Fax: 703-836-6086
Email: boblaw424@aol.com

Dominic Lee
Materials Scientist
Metals and Ceramics Division
Oak Ridge National Laboratory
Building 4500S, MS-6116
P.O. Box 2008
Oak Ridge, TN 37831-6116
Phone: 865-241-0775
Fax: 865-574-7659
Email: leedf@ornl.gov

Hee-Gyoun Lee
Senior Materials Scientist
SuperPower, Incorporated
450 Duane Avenue
Schenectady, NY 12304
Phone: 518-346-1414, Ext. 3044
Fax: 518-346-5622
Email: hlee@igc.com

Donald Liebenberg
Specialist
ORISE
49 Starboard Tack Drive
Salem, SC 29676
Phone: 864-944-7175
Fax: 864-944-5162
Email: liebenbergd@prodigy.net

David Lindsay
Manager, Superconductivity
Southwire Company
Cofer Technology Center
111 Development Drive
Carrollton, GA 30119
Phone: 770-832-4916
Fax: 770-832-5017
Email: david_lindsay@southwire.com

Beihai Ma
Research Scientist
Argonne National Laboratory
9700 South Cass Avenue
Argonne, IL 60439
Phone: 630-252-9961
Fax: 630-252-3604
Email: bma@anl.gov

Kenneth Marken
Project Manager
Oxford Instruments Superconducting
Technology
600 Milik Street
Carteret, NJ 07008
Phone: 732-541-1300
Fax: 732-541-7769
Email: ken.marken@ost.oxinst.com

Victor Maroni
Department Head
Argonne National Laboratory
Building 205
9700 South Cass Avenue
Argonne, IL 60439
Phone: 630-252-4547
Fax: 630-252-9373
Email: maroni@cmt.anl.gov

Dean Miller
Materials Scientist
Materials Science Division
Argonne National Laboratory
7826 Nantucket
MSD-212
Darien, IL 60561
Phone: 630-252-4108
Fax: 630-252-7777
Email: miller@anl.gov

Charles Oberly
Physicist
Wright-Patterson Air Force Base
Air Force Research Laboratory
AFRL/PRPG
1950 Fifth Street
Wright-Patterson AFB, OH 45433
Phone: 937-255-4814
Fax: 937-656-4132
Email: charles.oberly@wpafb.af.mil

Mariappan Paranthaman
Senior Research Staff
Oak Ridge National Laboratory
1 Bethel Valley Road
Building 4500 South, Room S-244
Oak Ridge, IL 37831-6100
Phone: 865-574-5045
Fax: 865-574-4939
Email: paranthamanm@ornl.gov

Dean Peterson
Center Leader
Los Alamos National Laboratory
STC MS K763
Los Alamos, NM 87545
Phone: 505-665-3030
Fax: 505-665-3164
Email: dpeterson@lanl.gov

Timothy Peterson
Research Leader
Air Force Research Laboratory
AFRL/MLPS
3005 Hobson Way
Wright Patterson AFB, OH 45433
Phone: 937-255-4474x3235
Fax: 937-255-4913
Email: timothy.peterson@wpafb.af.mil

Marshall Reed
Superconductivity Program
U.S. Department of Energy
1000 Independence Avenuenue, S.W.
Washington, DC 20585
Phone: 202-586-8076
Fax: 202-586-5860
Email: marshall.reed@hq.doe.gov

Kamel Salama
Professor
TCSAM
University of Houston
Houston, TX 77204-5002
Phone: 713-743-4514
Fax: 713-743-4513
Email: ksalama@uh.edu

John Scudiere
General Manager, Advanced Conductors
American Superconductor Corporation
Two Technology Drive
Westborough, MA 01581
Phone: 508-836-4200
Fax: 508-836-4848
Email: jscudiere@amsuper.com

Venkat Selvamanickam
Program Manager, Materials
SuperPower Incorporated
450 Duane Avenue
Schenectady, NY 12304
Phone: 518-346-1414, Ext. 3097
Fax: 518-346-6080
Email: vselva@igc.com

Shara Shoup
Director
MicroCoating Technologies
5315 Peachtree Industrial Boulevard
Chamblee, GA 30341
Phone: 678-287-2478
Fax: 678-287-3999
Email: sshoup@microcoating.com

Masaki Suenaga
Senior Scientist
Brookhaven National Laboratory
76 Cornell Avenue
Building 480
Upton, NY 11973
Phone: 631-344-3518
Fax: 631-344-4071
Email: mas@bnl.gov

Stephen Umans
Consultant
Rockwell Automation
MIT Room 4-205
Cambridge, MA 02139
Phone: 617-253-7351
Email: umans@mit.edu

James Voigt
Professional Member of Technical Staff
Sandia National Laboratories
MS-1411
Albuquerque, NM 87185-1411
Phone: 505-845-9044
Fax: 505-844-9781
Email: javoigt@sandia.gov

David Welch
Senior Scientist
Materials Science Department
Brookhaven National Laboratory
76 Cornell Avenue
Building 480
Upton, NY 11973-5000
Phone: 631-344-3517
Fax: 631-344-4071
Email: dwelch@bnl.gov

Philip Winkler
Manager, Government Systems
Air Products and Chemicals, Incorporated
7201 Hamilton Boulevard
Allentown, PA 18195
Phone: 610-481-4284
Fax: 610-481-2576
Email: winklepw@apci.com

Alan Wolsky
Senior Scientist, Operating Agent for IEA HTS Impl.
Energy Services Division
Argonne National Laboratory
9700 South Cass Avenue
Building 362
Argonne, IL 60439-4815
Phone: 630-252-3783
Fax: 630-252-1677
Email: awolsky@anl.gov

Yi-Yuan Xie
Materials Scientist
SuperPower, Incorporated
450 Duane Avenue
Schenectady, NY 12304
Phone: 518-346-1414
Fax: 516-346-6080
Email: yxie@igc.com

Xuming Xiong
Senior Materials Scientist
SuperPower, Incorporated
450 Duane Avenue
Schenectady, NY 21034
Phone: 518-346-1414
Fax: 518-346-6080
Email: xxiong@igc.com

APPENDIX: YBCO COATED CONDUCTOR ISSUES

YBCO COATED CONDUCTOR ISSUES

The development of coated conductors has reached a critical juncture, whereby on the one hand, the first coated conductor tapes beyond a 10-m length are being produced, while on the other hand, the field continues to broaden in terms of materials and techniques being developed. The workshop aims to assess long-term and short-term goals and needs, starting from an evaluation of the current status for each of the components of a typical YBCO coated conductor, i.e. the metallic substrate, buffer layers, and the YBCO coatings. In addition, we will also focus on the issues towards application and characterization of coated conductors. The speakers are asked to address a number of issues formulated by the organizers and provide their views in their presentation. Each presentation is limited to 10 min. There will be no question period after the presentations, however, at the end of each session, the issues will be discussed as a whole in the context of the multiple views presented.

The following contains a listing of the questions/issues to be addressed for each session. The presenter is asked to comment only on the issues particular to his/her topic and the associated session. Issues not included in the list but considered equally or more important also may be discussed.

Issues related to YBCO film growth:

- **Current Status**
  What is the best performance (I_c/cm-width) that can presently be achieved with your process on coated conductor substrates? What is the YBCO thickness, I_c (A/cm-width), J_c?
  What is the performance using currently preferred processing parameters for long length production, taking into account production rate, reliability, etc.? In other words, what is the best compromise now for making a long tape (> 100 m) with reasonably high I_c? What is the YBCO thickness, I_c (A/cm-width), J_c, production rate for this compromise condition?
- **Scale-up: next level**
  What is the maximum length (area) that can presently be produced in a single run (before regeneration of equipment/sources is required)? How can process continuity be maintained beyond regeneration limits?
  What is the most sensible, near-term scaling-up step towards: a) higher I_c/cm-width, and b) higher production rate? What obstacles need to be overcome to bring the process to this near-term, higher level?
- **Scale-up: long term**
  What are the advantages of your technique for the fabrication of long-length YBCO coated conductors? Assess which advantages are unique.
  What are key issues for large-scale production? Describe pathways for future development. Indicate research and technological needs. Describe a level of development at which your technique may be available for prototype demonstrations requiring: a) > 100 m of tape, b) > 10 km of tape (I_c > 150 A at 77 K).

Issues related to Substrate/buffers (IBAD, ISD, RABiTS, ITEX):

- **What is the current status of your substrates?**
  The typical texture that can be readily obtained in short samples
  The typical texture and uniformity that can be readily obtained in longer samples (up to a meter)
  Typical texture and uniformity that can be readily obtained in longer samples (10-100m)
  Typical texture obtained in wide samples (at least several cms to several inches)
- **What are your process characteristics?**
  Speed of the process
  What is limiting the degree of biaxial texture? How can it be improved?
- **What are the intrinsic issues?**
  Surface finish requirements (cleaning, polishing, etc.) and how they are being met?
  Effect of surface finish intrinsic to texture development? Or merely to growing thick epi YBCO films?
  Strength and magnetism of substrate issues
  Mechanical properties of substrate
- **What are the future prospects (in the next one year)?**
  What would be most difficult aspect of the process to scale up to long lengths of 100m?
  What would be most difficult aspect of the process to scale up to wide lengths of several inches?
  What research areas do you think need focus in order to make this substrate technology viable?

Issues related to New Buffer Layer Technology:

- **What is different about your process with respect to other standard Physical Vapor Deposition (PVD) techniques?**
- **What is the economics of your process?**
  This includes speed, simplicity, minimum buffer layer thickness, processing issues, deposition rates, etc.
- **What is the current status of the performance of your buffers?**
  What YBCO deposition technique was used? How long, how wide, how fast, and how good can you make?
- **What are the near-term problems that need to be resolved?**
  This includes starting chemicals, furnace designs, process conditions, reproducibility, interaction of buffers with YBCO, substrate surface conditioning, stress related issues, etc.

Issues for applications of Coated Conductors:

- **Why would coated conductor be preferred for this application?**
- **What is your operating field, temperature?**
- **Desired conductor cost at that field, temperature: from 2005 - 2010**
- **Preferred amperage of conductor (is there a maximum?): from 2005 – 2010**
- **Preferred conductor width and thickness (including parallel shunt if needed)**
- **Single piece lengths required**
- **Properties that include all of these, but not limited to**
  n value at operating conditions
  Engineering J_c including parallel shunt
  Bend strain for 10% reduction in J_c
  Tensile strength at 10% reduction in J_c
  a.c. losses at operating conditions
  Joint resistance
  Uniformity in J_c
  Magnetic properties (esp. in consideration of substrate)

Issues related to the characterization of coated conductors:

- **Describe microstructural issues of YBCO coated conductors that are most urgent for future progress.**
- **Reel-to-reel transport property measurements. What are the issues and how can they be addressed?**
- **Discuss quenching and thermal stability studies related to YBCO coated conductors.**
- **AC losses. What the tape geometry and ac loss measurement issues? Design aspects, ellipse model or strip model, etc.**
- **What are the advantages and disadvantages of coated conductors compared to BSCCO and MgB_2 conductors?**
- **Effect of defect distribution on I_c incorporating all the theoretical aspects. What are the most important aspects of both primary and secondary levels of defects? Effect of grain size, pinning centers, etc.**
- **What are the in-situ diagnostics that need to be looked into for RABiTS, IBAD, etc? Also include YBCO ex-situ & in-situ processes.**

Session: YBCO by Pulsed Laser Deposition

1. **Herbert C. Freyhardt (Univ. of Goettingen)**
   High Rate PLD + IBAD-YSZ
   10 meter, > 200 A/cm, >2 MA/cm^2, 65-70 nm/min, 1.3 m/h @ 4 mm width
   FCL: 2500 – 5000 A max 55 f-500L tube YBCO
   PLD=High Reproducibility

2. **Yasuhiro Iijima (Fujikura Ltd.)**
   PLD + IBAD-Gd2Zr2O7
   30 meter, ~ 1 MA/cm2, 40 A, 0.5 m/h
   - **needs improvement on**
     - **Temperature control, F_2 gas recharge, target degradation,**
     - **YBCO collection yield (few % to 30-50 %…)**
     - **® W-laser, target automatic changer, …**

3. **Kazuya Ohmatsu (Sumitomo Ltd.)**
   PLD HoBCO + ISD-YSZ, CeO2
   High Power Large PLD system; 200 W laser, 250 f-target
   10 meter, 0.2 MA/cm^2, 5 m/h
   50 meter, CeO_2 buffered Ni metallic tape
   To achieve 50 meter HoBCO tape within the end of 2002

4. **Dean Peterson (Los Alamos National Laboratory)**
   PLD + IBAD MgO
   Multi-layer structure SmBCO/YBCO
   Thicker and High Ic Conductor
   1 meter, > 200 A/cm on IBAD-YSZ
   600 A/cm short sample

5. **Hans Christen (Oak Ridge National Laboratory)**
   Cost of laser
   ® $33/kA-m at demonstrated values (LANL, Goettingen, Fujikura, 2001)
   ® $12/kA-m by increase in laser device ability such as collection efficiency ….
   ® $3.5/kA-m by Jc increase to 2.5 MA/cm2 and laster tube price 50% down

   Cost standard $ 50/kA-m

Presenter			Lee(ORNL)	O'Neil(3M)	Suenaga (BHNL)	Feenstra (ORNL)	Yoshizumi (MIT)	Izumi (ISTEC)	Verebelyi (AMSC)
Procesas			BaF2	BaF2	BaF2	BaF2	TFA	TFA	TFA
Current Status	Ic*A/cm-w & Thickness		90A/cm-w 0.82µm	45A(2m)	200A/cm-w 5µm/on YSZ-Ni	270A/cm-w 3µm	96A/cm-w 0.8µm	153A/cm-w 1µm	118A/cm
	Compromise Conditions for Long Tapes						Low? High(PH2O)		
Scale up Next Level	Max. Length		1m	15m		6m	0.6cm	10cm	1m
	Continuity							Coating.OK LowTemp.:? High Temp.:X	
	Seinsible Factors & Obstacles	High Ic	High PH20	Thick Film High quality conversion	Batch			Density & Thicker Film	thick YBCO better texture
		High Production Rate		Conversion Rate Evap. Rate		Batch & Large Area		Shorter Low Temp Anneal	
Scale up Long Term	Advantages of Your Tech. for Long Tapes		Low Pressure	Dense Precursor RTR			High Growth Rate & Texturing	Multi: Coating, New Solution: Shorter Time?	High Yield, No high vac system
	Key Issues (Pathway)		Homogeneous YBCO , HF Handling	Uniformity Conversion rate		Comp. Control	Flat and Uniform Precursor	Comparison in Batch & RTR	performance & cost over BSCCO
	Prototype		100m/h 5-10m 200A		1000A/cm-w	100m/h 4mm-w 5µm YBCO		300A/cm-w, 500m,5m/h	

Speakers	Shiohara	Strikoviski	Hammond	Lee	Kashima	Donet
Process	LPE	PED	in-situ e-beam evap	MOCVD	MOCVD	MOCVD
Buffer	SOE	Rabits	LaO	IBAD	untextured Ag/ {110}<110>textured Ag	SOE
Best Ic	> 100 A/cm	34 A/cm	150 A/cm	150 A	3.2 A on textured Ag	
YBCO thickness	1 micron	0.4 micron	0.7 - 1 micron	1.2 micron		
Best Jc	1 MA/cm2	0.85 MA/cm2	2.5 MA/cm2	1.3 MA/cm2	0.55 MA/cm2 on textured Ag	0.86 MA/cm2
Long length best performance				90 A over 1 m	2.5 A ; 61,000 A/cm2 over 100m on untextured Ag	
Maximum length before regeneration of sources	Lifetime of crucibles	lifetime of electron sources	rod feed sources in scale up mode (can produce kilometers)	Unlimited ; precursors outside deposition chamber ; no regeneration limits for sources		
Scale up for higher Ic	high crystallinity ; Long oxygen anneal	better understanding of PED process	higher rates (350 Angstroms/s) can possibly lead to higher Jc (5 MA/cm2)	Need better Jc in thicker films (roughness, sec. Phases, texture need to be improved)	Better substrates	
Scale up for higher rate	1 micron/min possible, but low Jc; abandoning LPE for now	Array of PED sources ; 13 * 2 array built in Germany	6000 km/yr possible at 100 Angstroms/s , L = 30 cm, w = 1m ; may possibly increase up to 1000 Angstroms/s	To demonstate high throughput with longer showerhead	6-stage CVD reactor set up ; only process used to produce 100 m YBCO ; 10 m/h demonstrated	4 m/h now ; Jipelec reactor has 45 cm2 area ; tape speed 40 m/h possible
Obstacles	high crystallinity ; Long oxygen anneal	Higher Jc ; more robust & reliable source	need O2 sensor	high Jc in thick films	Better substrates	
Advantages	High throughput at high temperature	1/10 cost of PLD ; small footprint ; better energy efficiency	high deposition rates (1000 Angstroms/s possible) ; Jc could be independent of thickness	High rate & unlimited deposition area	High throughput	Modular ; can easily add modules for high throughput
Research & Technological needs	Need architecture that yields high growth rate & high Jc		need to transfer technology to metal substrates - need to lower operating temp and/or high temp buffers	Further improvement in precursors		

Presenter			Groves (LANL)	Iijima (Fujikura)	Berdahl (LBNL)	Ohmatsu (Sumitomo)	Balachandran (ANL)
Process			IBAD(MgO)	IBAD(YSZ,GZO)	ITEX(YSZ)	ISD(YSZ,CeO2)	ISD(MgO)
Current Status	Short(buffer/YBCO/Jc)		6°/2°/	10°(7)/7°/1.7MA/cm2	broad/broad/0.25M	18°/14°/0.27M	10°/13°/0.55MA/cm2
	1m(buffer/YBCO/Jc)		8°/3°/	10°/7°/1.0MA/cm2		20°/16°/	12-18°/0.35 M
	10-100m(buffer/YBCO/Jc)			10-14°/7-11°/0.8-1M		23°/19°/	
	Wide(buffer/YBCO/Jc)		Double width 8.2?				
	Max Length with reasonable		1m	60m	short	50m	
Process Characte-ristics	Texturing	Limitting Factors	MgO critical thickness substrate roughness	Trade off with Speed	?	ISD buffered layer	12-18° in moving tape(0.35M)
		How to improve?	use of nucleation layer polishing technique	Beam Control, Cap Layer	basic optimization	Reverse ISD, Cap Layer on ISD	Thickness control, reverse ISD
	Speed	Limitting Factors	5m/h	Now 0.5-1.0m/h Trade off with Texturing	3nm/s	Now 0.2-0.5m/h Rate of Ho123	20-100A/sec Growth rate
		How to improve?	increase deposition area	Large Area Depo. Materials, CeO2	straight forward	Improve optical system	Increase dep.area/larger reel-to-reel chamber
	Grain Size		5nm	5-10nm	20-200nm	50nm	approx. 0.2 micron
Intrinsic Issuers	Effect of Surface (Sub? Buffer/Buffer? YBCO)		texture of buffer/ lattice matching	Very Smooth	may not need smooth sustrate	20nm is required afffected	Need to make ISD layer smooth
Future Prospect	Obstacles	for 100m	non expected	Nothing		Buffered Layer Development	No obstacle-Equipment for reel to reel deposition
		for several inch width	reduction of gun divergence	Nothing		Size of YBCO (HoBCO) Plume	Reduction of beam divergence
	Research Area		IBAD Mechanism	Mechanism of Texturing	amorphous YSZ synthesis YBCO deposition on YSZ	Improvement ISD, New Buffer Layer	roughness control, uniform thickness

Speakers	Peterson	Sathyamurthy	Shoup	Matsumoto	Aytug	Sambasivan
Buffer layer	SrRuO3	La2Zr2O7	SrTiO3/CeO2	BaSnO3, BaZrO3	LaMnO3	YZN
	on MgO IBAD/Ni-alloy	on textured Ni-W	on textured Ni	on SOE NiO/Ni	on textured Ni-W	on Ni or Ni-Cr13%
Process	PLD	solution	CCVD	PLD, MOD Solution	rf sputtering	reactive sputtering
Economics		low-cost; good diffusion barrrier for Ni	non-vacuum, long length, low capital & materials cost, no post-annealing	non-vacuum, high speed	good diffusion barrier for Ni	ECONO process; Epitaxial Conversion to Oxide via Nitride Oxidation
Speed		double-sided	5 h/m	1-10m/hr		1 m/min (feasible) but not demonstrated yet
Simplicity	single cap buffer	single -buffer for PLD YBCO; CeO2 cap for TFA/BaF2				YZN to YSZ; CeO2 cap
Minimum buffer thickness	50 nm (continuous)	60 nm	240nm (200nm, 40nm)		60 nm (300 nm for thick YBCO)	70 nm YZN to produce 100 nm YSZ (volume increases)
Reproducibility						
Processing issues	no chemical reaction with MgO IBAD layer or YBCO	BZO formation (CeO2 cap layer), substrate surface conditioning (sulfur), furnace design to emulate spin-coating		rough surface; Ra > 20 nm; low Jc YBCO on Ni-W	Jc on Ni-W is little lower than standard buffer architecture	O2 control
Current status		1 cm wide; up to 25 cm long	< 3m length			5 meter long buffers
YBCO performance	1.8 MA/cm2 (1.1um); 1.7 MA/cm2 (1.3 um)	Ic of 80A,	1 MA/cm2 (0.2 um)	0.45 MA/cm2 (0.5 um) on PVD BaSnO3; 0.89 MA/cm2 (0.4 um) on PVD BaZrO3; 0.36 MA/cm2 on MOD BaZrO3	1.3 MA/cm2 on LMO (60 or 300 nm)/Ni-W; 0.9 MA/cm2 BaF2 YBCO/LMO/Gd2O3/ Ni; Ic 230 A/cm for LANL YBCO (1.65 um)/LMO/LANL IBAD-MgO/Ni-alloy	1 MA/cm2 TFA or PLD YBCO on YSZ/NiCr; 1MA/cm2 PLD YBCO/MgO/TiN/Ni
What tech.?	PLD	reel-to-reel dip-coating	PLD	PLD	PLD	PLD
How long, wide, fast, and how good	short samples	25 cm long solution buffer	up to 3 meter; 1 cm wide		short samples	short samples
Near-term problems	depo T , thickness to be optimized, Goal: Ic > 100 A/cm on 1-meter SRO/IBAD MgO/Ni-alloy	single -buffer for PLD YBCO; CeO2 cap for TFA/BaF2		need mechanical polishing	large area LMO targets, increase throughput	

Characterization of Coated Conductors Session Summary

A) Non-destructive quality control

1) Process monitoring

For this purpose, the applications of Raman and Auger spectroscopy techniques were presented. The former is for detecting defects, such as antisite and oxygen deficiency, in the finished YBCO tapes while the latter is for the reel-to-reel detection of S coverage on the surface of RABiT-Ni substrates. This is needed to ensure the epitaxial deposition of CeO_2 or Y_2O_3 seed layers on Ni. Also, the former was being developed for in situ monitoring of YBCO formation. If this is accomplished, this will be very valuable for YBCO long tape production, which employs, for example, MOCVD for YBCO deposition.

2) Local J_c distribution

Possible use of magneto-optical imaging of J_c distribution was proposed for the reel-to-reel detection of low J_c regions of long tape. However, a better use of this technique is likely to be in conjunction with a standard reel-to-reel I_c measurement of superconducting tapes by transport currents to examine only the "bad" spots of the tapes in detail. Such I_c measurements are already being used for quality control of Bi2223/Ag tapes.

B) TEM

1) The importance of TEM in revealing the role of the interfacial reaction in the epitaxial YBCO nucleation as well as the retainment of the c-axis orientation during the growth was pointed out. Also, the in- and out-of plane local misorientations among the grains can be nicely determined by the use of selected area diffraction technique as well as dark field imaging in TEM. However, the most important use of TEM is to identify and separate the process and the materials related microstructures, and then one can relate the microstructures and the properties with the processing variables.

C) Electromagnetic Properties:

1) Electro/thermal stability

As the critical currents of the tapes become increasingly large, the so-far neglected investigation of the cryo-stability of the coated conductors will become an important issue. At this moment, a good theoretical modeling is badly needed to assist better understanding of the limited available experimental results.

2) dc critical currents and ac loss characterization and modeling.

Very nice models of dc critical currents and ac losses were presented. The next step needed is to develop the identification of the microstructural defects, which lead to the modeled dc or ac loss behaviors.

Organization	Sinha Southwire	Barnes Air Force	Ishiyama Waseda Univ.	Kashima Chubu	Malazemoff AMSC	Neumueller Siemens	Shiohara ISTEC
Application	cable	generator transformer	SMES	cable	generator motor wind turbine gen	FCL	MagLev
Why coated Conductor?	cost	low ac loss, high T high Ic	reduce coil volume incr. refrigeration eff.		cables magn.processing	fast switching strong limiting	
T (K), B(T)	72-77 self-field	4-5 T, 20-77	incr. Stability 50 K, 10-T				
Cost ($/kA-m))	<50	not so cost-sensitive	<NbTi	<50	<50	<100	10 at 50 K
I (A/cm); maximum I?	50 min	20 to 300 (DC) 1 MA	1 to 10 kA (50 tapes) 12 coils (toroid)	Je=0.07 MA min.		100 A/cm	40 kA/cm^2 at 5T, 50 K
width (mm)	3 to 5			3 to 4		10 mm	
thickness (mm)	0.15-0.2					0.2	
Length (m)	200	2000		300-500	40	100	1000
Mechanical Properties	higher than BSCCO			1.2 E6 A/cm^2		higher than BSCCO	
ac losses		generator: <100 W/MW				NA	
joint resistance							
needs		withstand 15,000 rpm 2-5 MW 100 A/turn L (2006-2010): 1000 km 2011-2015: 5000 km	(need transposed cable)	survive short-circuit 31.5 A cable length 150-200 m	refrigeration 50-55K	high Voltage per length	high thermal conduct. n>20